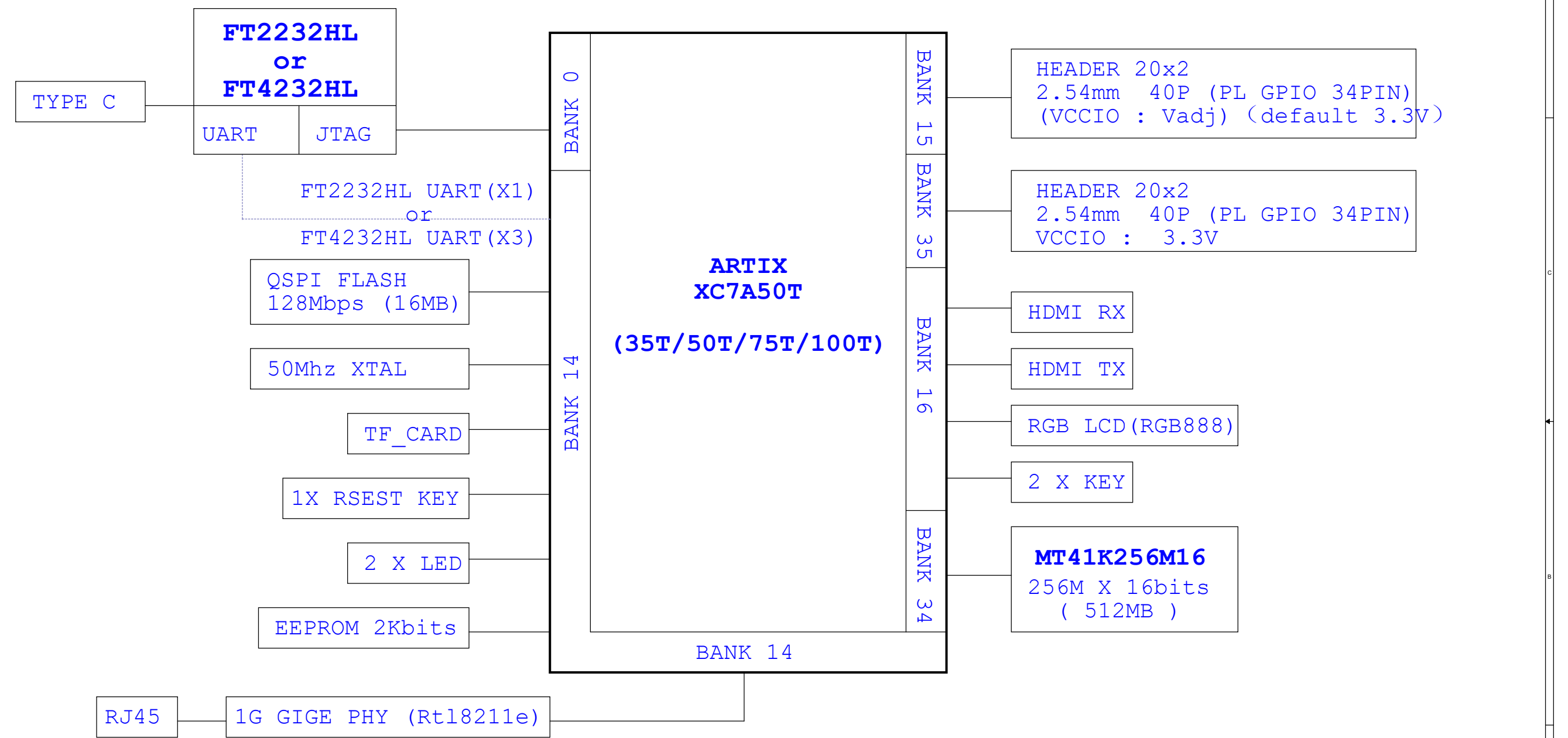


54321

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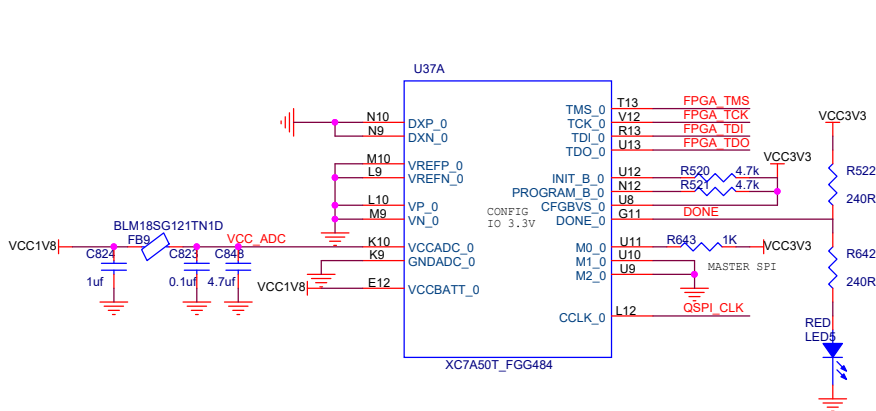
Smart Artix
Block Diagram

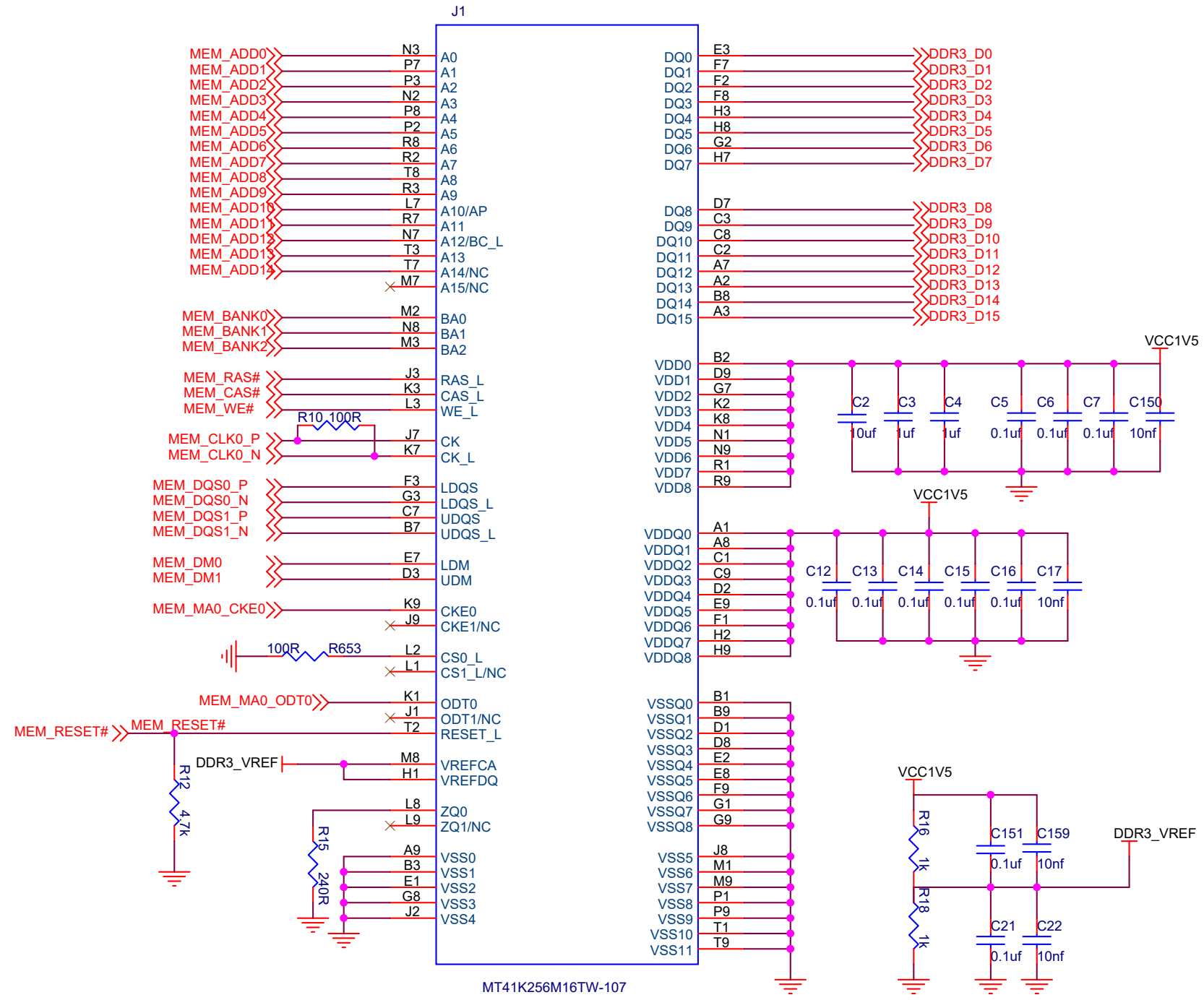
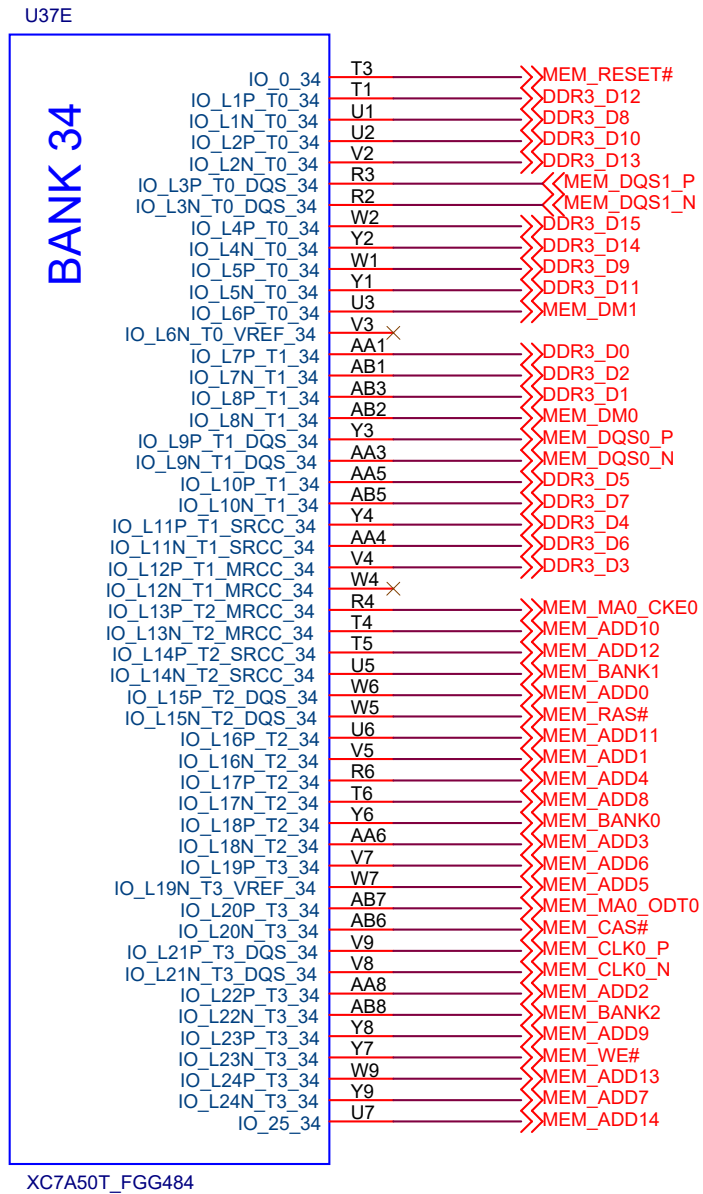
VER : 1.3



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VCCIO : BANK 15 Vadj (default 3.3V)
BANK 35 3.3V

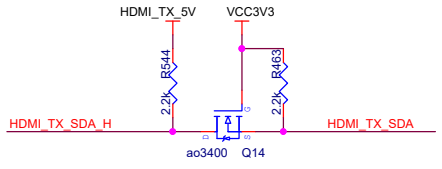
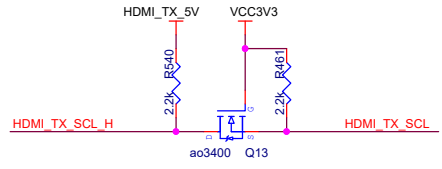
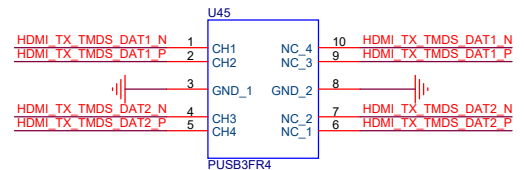
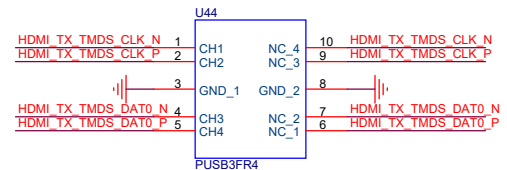
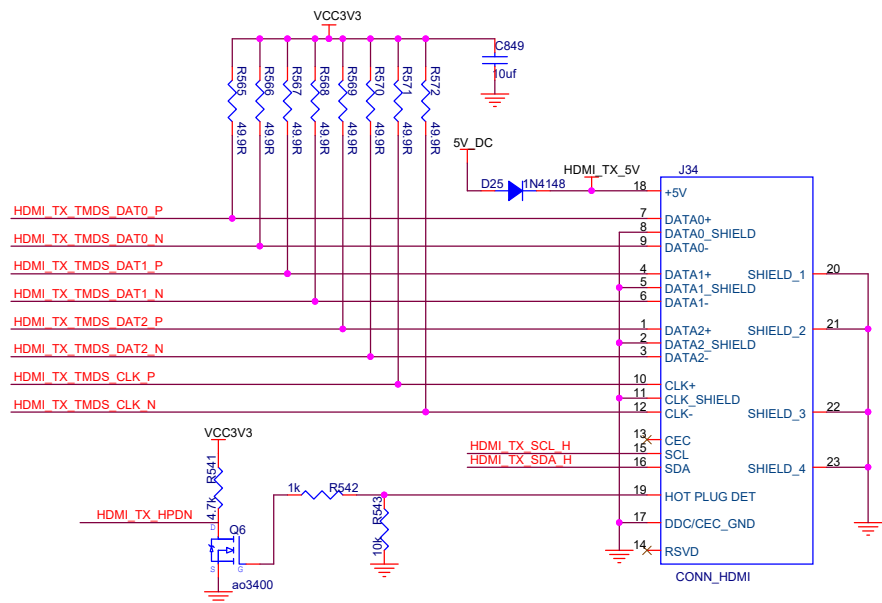




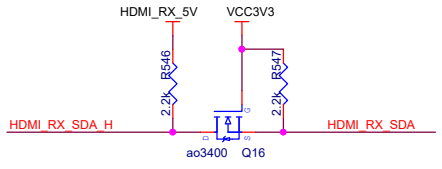
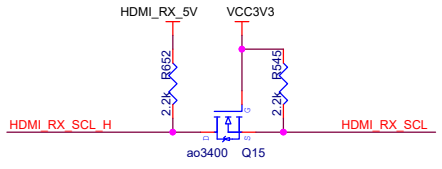
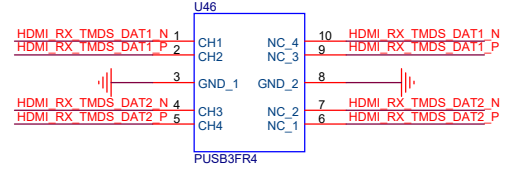
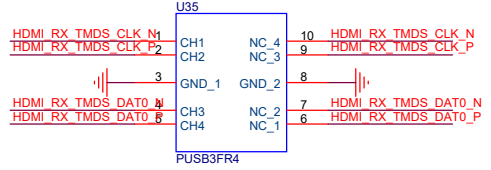
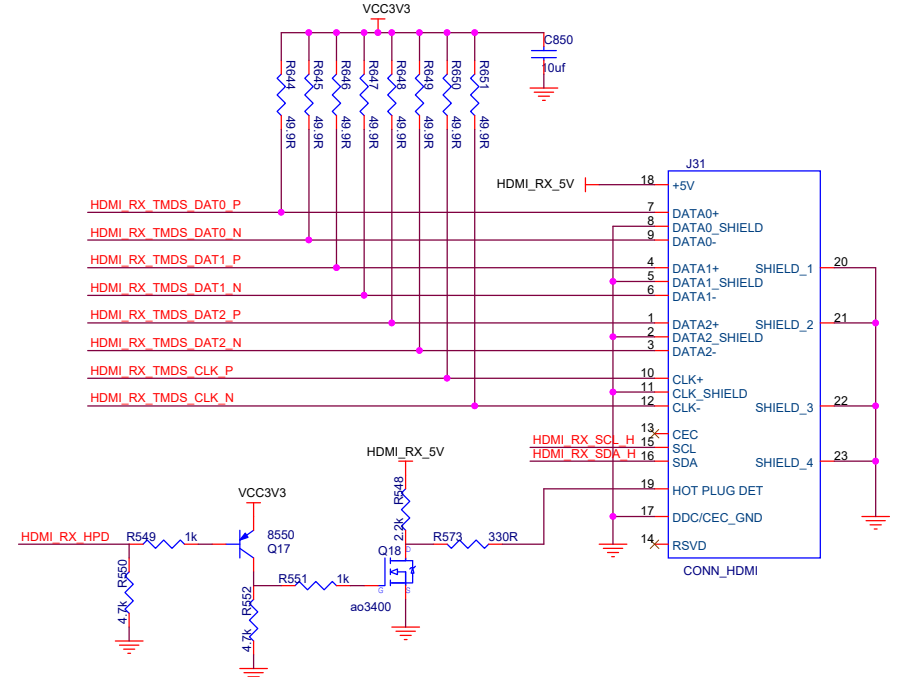
DDR PART

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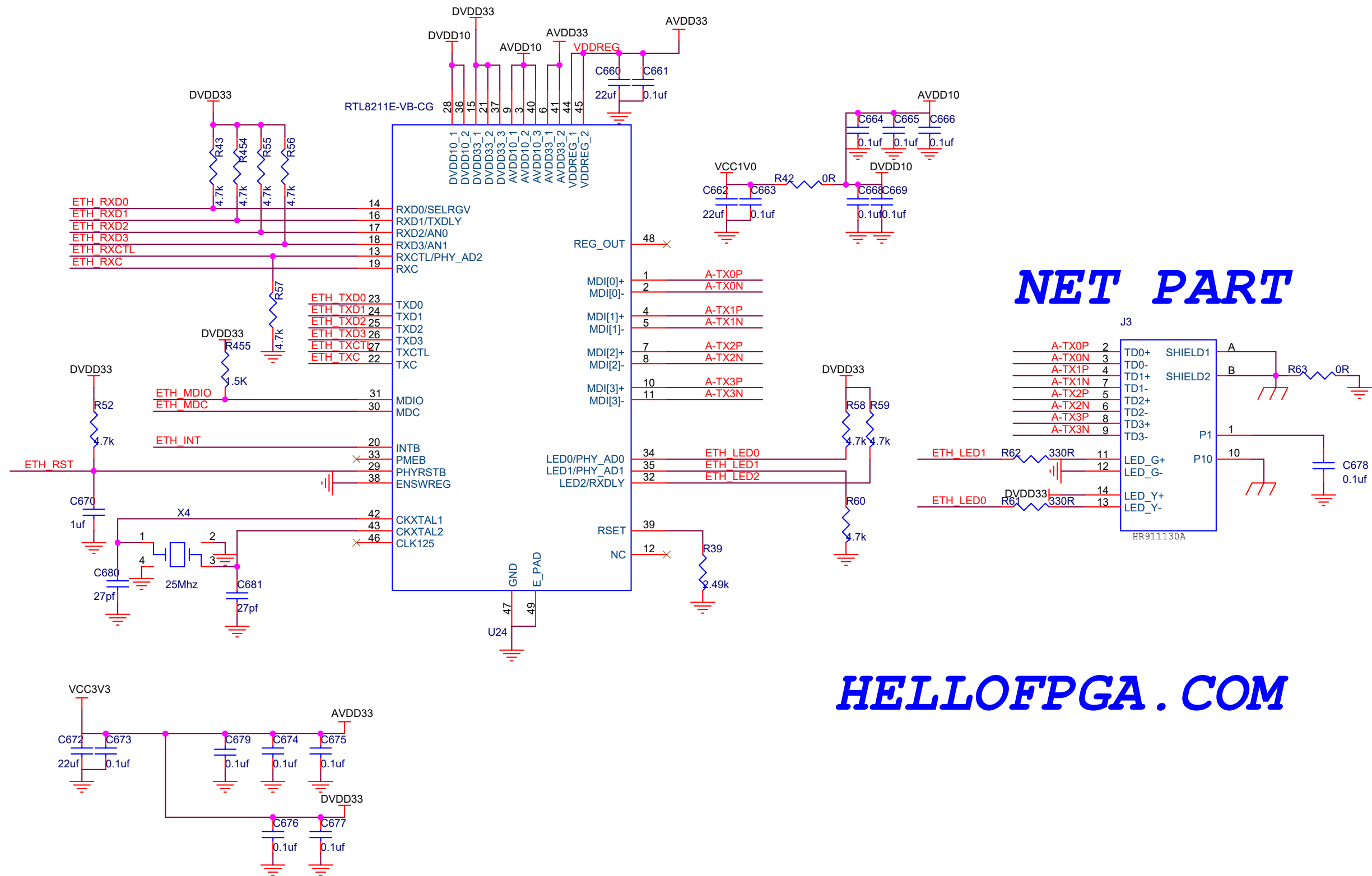
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Size	Document Number	Rev
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Date:	Thursday, November 13, 2025	Sheet 1 of 1



HDMI_TX



HDMI_RX

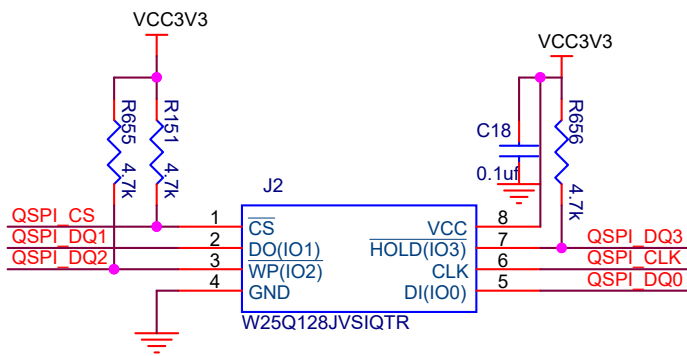


NET PART

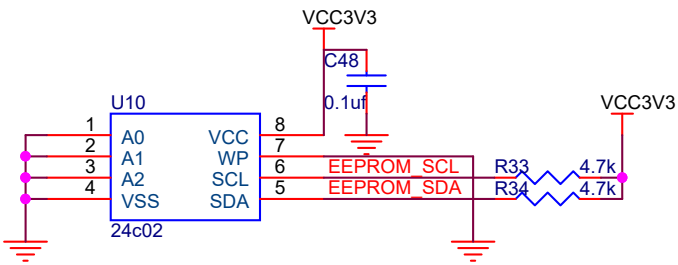
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Date:	Thursday, November 13, 2025	Sheet 1 of 1

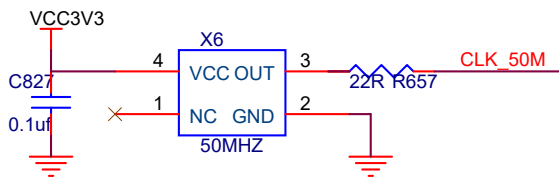
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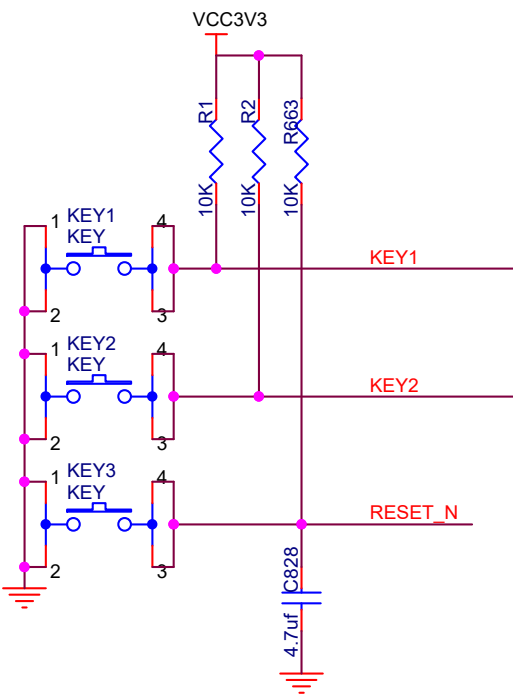
EEPROM



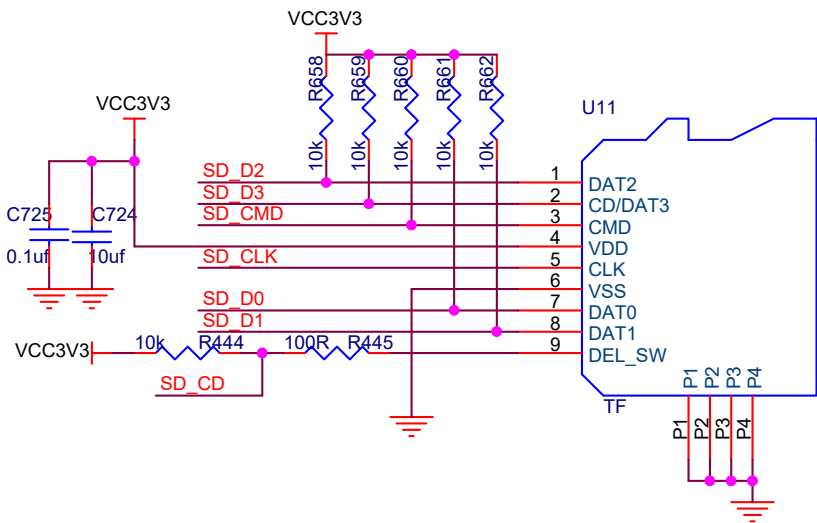
FPGA CLK



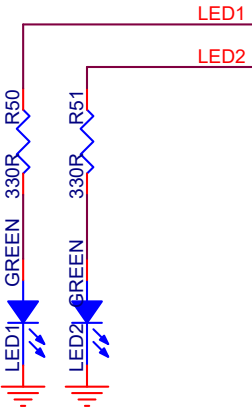
KEY



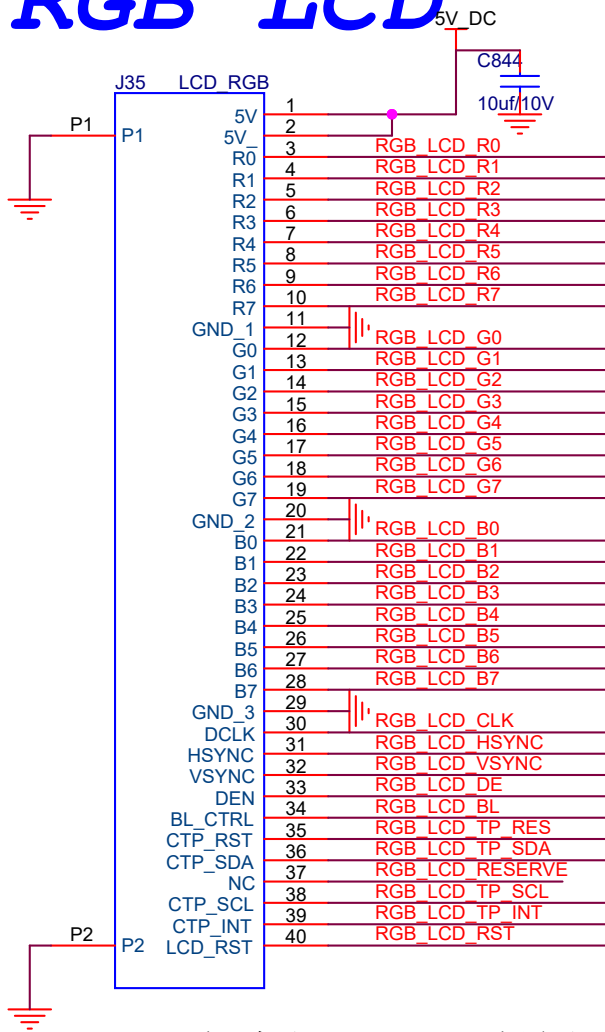
TF CARD



LED



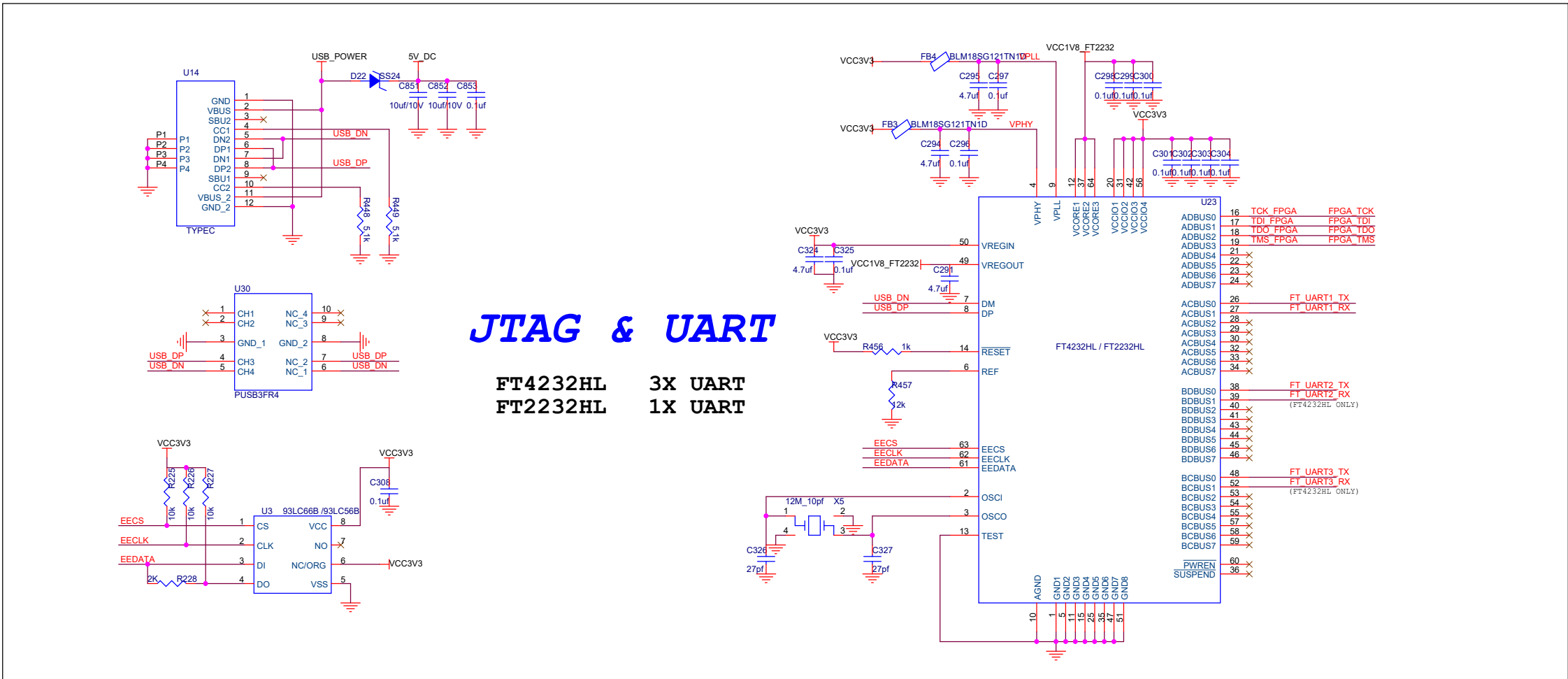
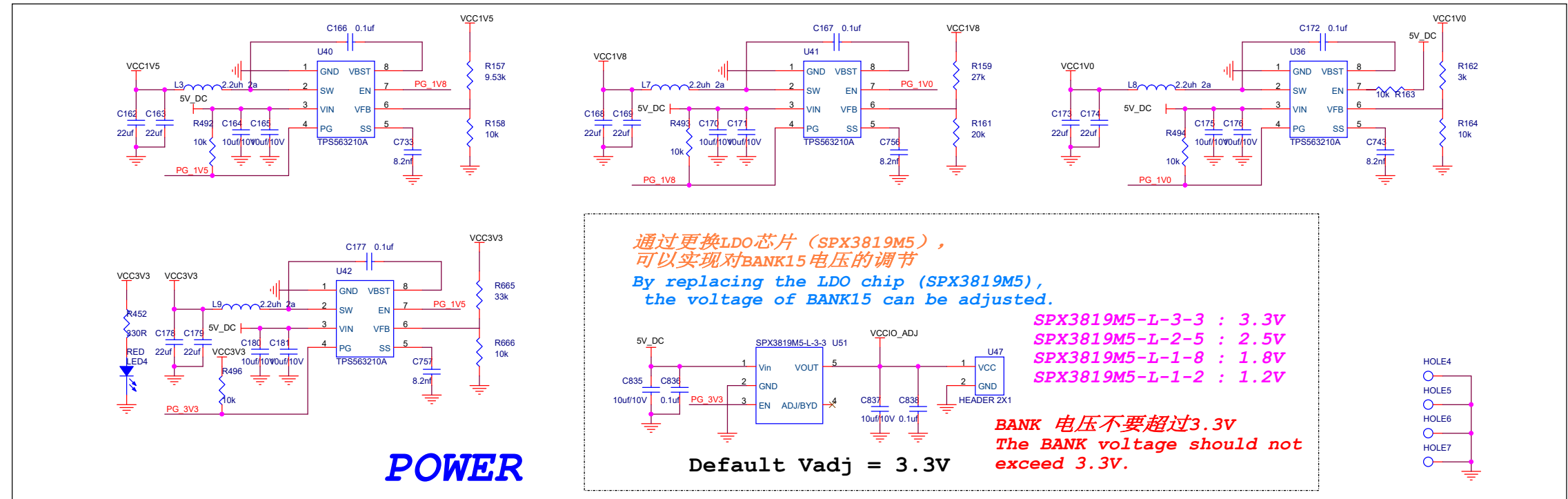
RGB LCD



FPC 适配本站RGB LCD & 正点原子40P LCD
RGB LCD Interface
RGB888

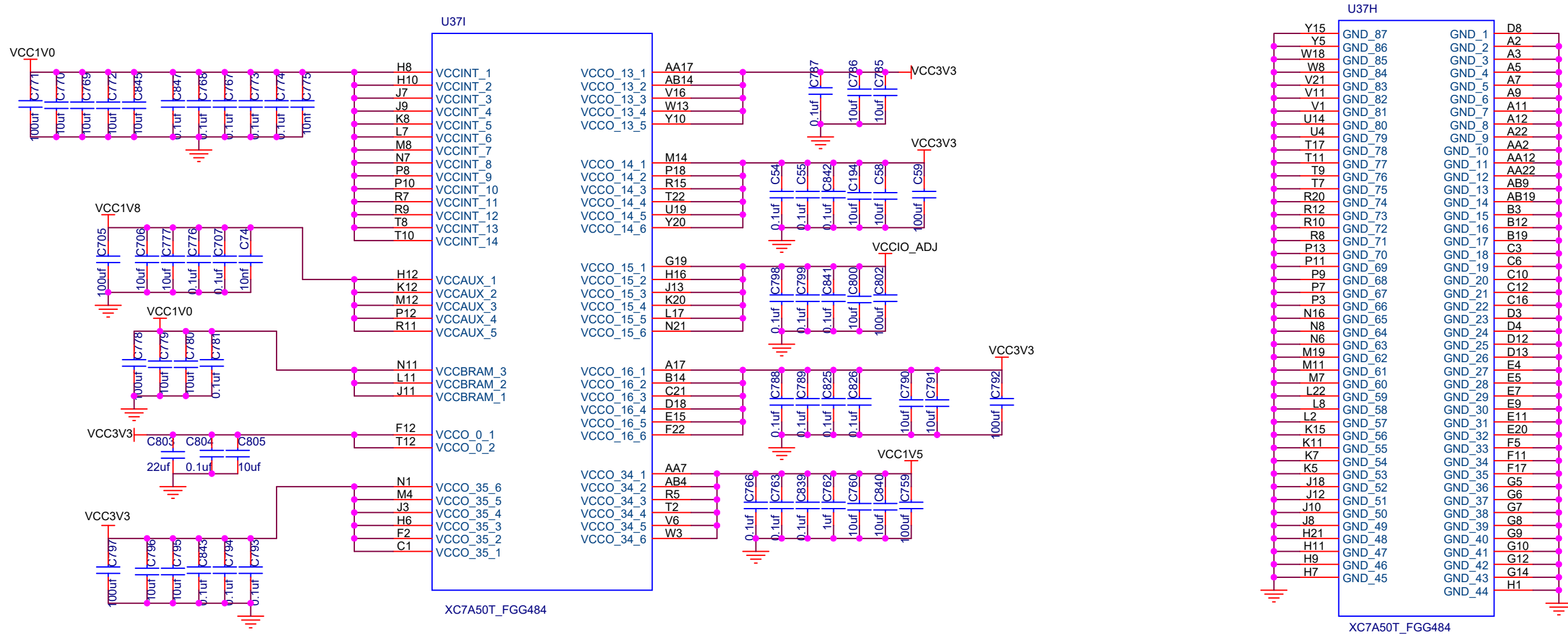
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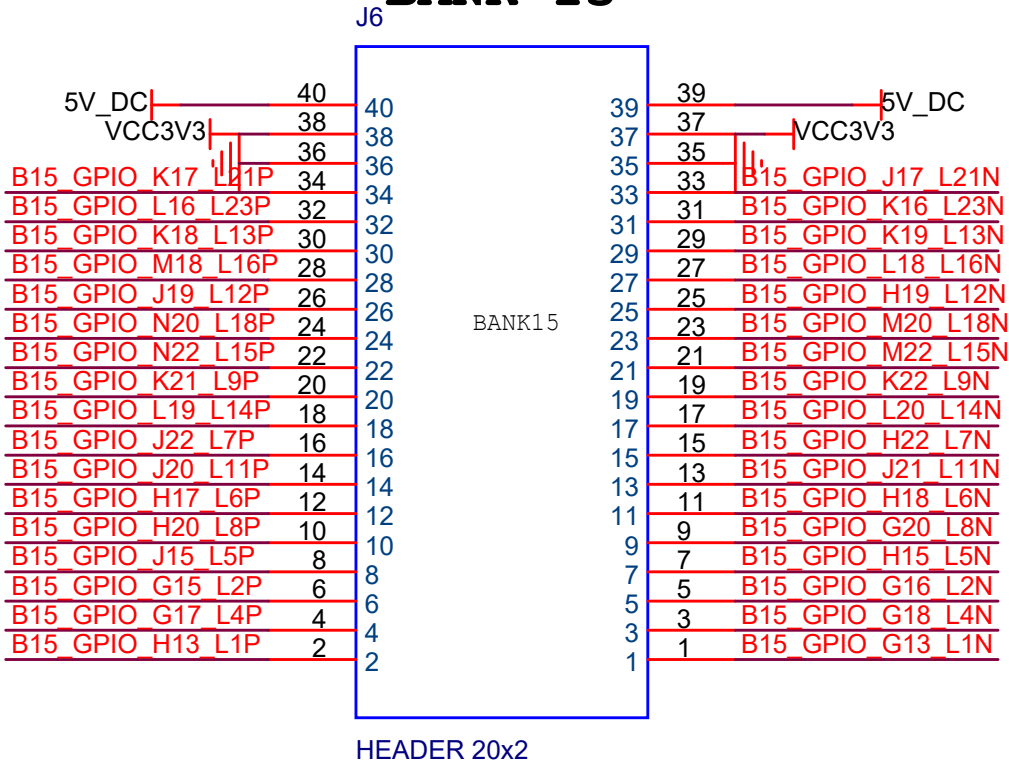
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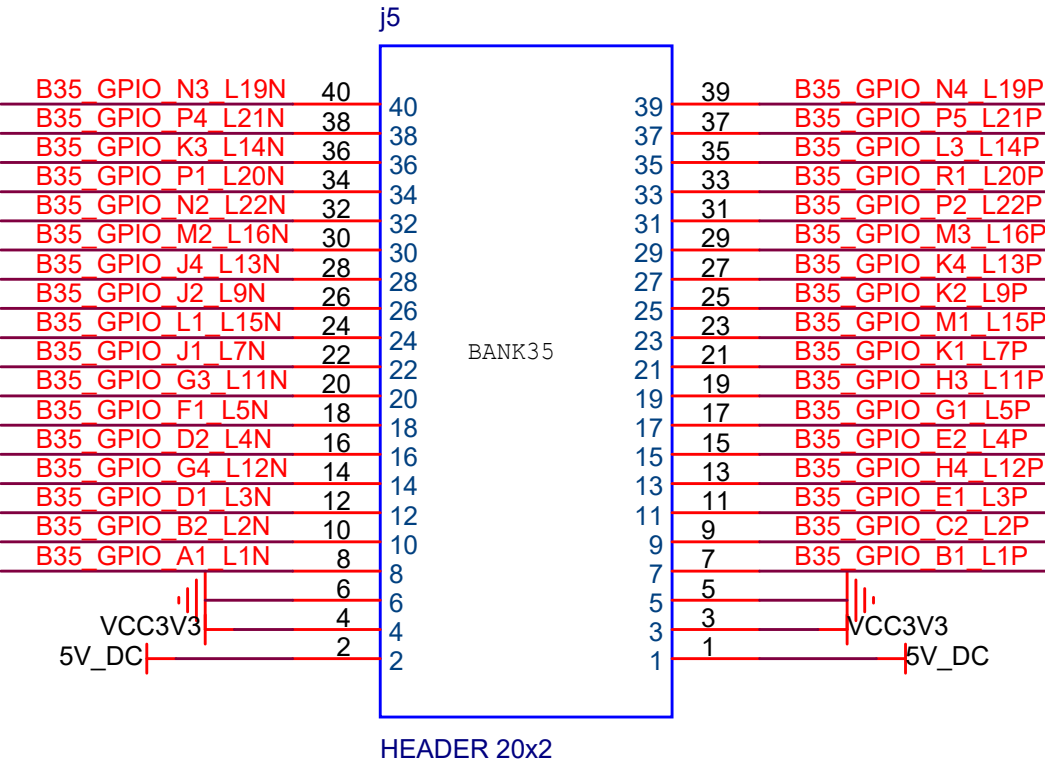
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BANK 15



VCCIO :VADJ
Default Vadj = 3.3V

BANK 35



VCCIO :3.3V

KEY & LED

KEY1	E22
KEY2	G22
LED1	R17
LED2	P16

RESET (KEY)

RESET_n (KEY3)	T20
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50M CLOCK

CLK	Y18
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HDMI

	RX	TX
CLK	C18	D17
D0	B21	C14
D1	B20	C13
D2	A18	E13
SDA	D15	N14
SCL	E16	N13
HPD	D16	N15

UART

TX1	R14
RX1	P14

TX2	P15
RX2	R16
TX3	U21
RX3	T21

(FT4232HL ONLY)

EEPROM

SCL	U18
SDA	T18

TF CARD

SD_D0	U20
SD_D1	V18
SD_D2	V22
SD_D3	Y21
SD_CMD	Y22
SD_CLK	V20
SD_CD	U17

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GigE phy

ETH_TD0	AB20
ETH_TD1	AA19
ETH_TD2	Y19
ETH_TD3	AB18
ETH_TX_CTL	AA18
ETH_TXC	AB21
ETH_RD0	AA20
ETH_RD1	W22
ETH_RD2	W21
ETH_RD3	W20
ETH_RX_CTL	AA21
ETH_RXC	W19
ETH_MDIO	V17
ETH_MDC	W17
ETH_INT	AB22
ETH_RST	V19

RGB_LCD

R7	E19
R6	E18
R5	F18
R4	E21
R3	F19
R2	F20
R1	F21
R0	G21
G7	D19
G6	D14
G5	F16
G4	D21
G3	F15
G2	F14
G1	E17
G0	F13
B7	B18
B6	B17
B5	A16
B4	A15
B3	A14
B2	B16
B1	A13
B0	B15
HSYNC	C20
VSYNC	D22
CLK	D20
DE	B22
BL	C22
RST (RESERVE)	R19

TP_RES	N17
TP_INT	P20
TP_SCL	R18
TP_SDA	P17

TOUCH

(RESERVE)	P19
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DDR

D0	AA1
D1	AB3
D2	AB1
D3	V4
D4	Y4
D5	AA5
D6	AA4
D7	AB5
D8	U1
D9	W1
D10	U2
D11	Y1
D12	T1
D13	V2
D14	Y2
D15	W2
AD0	W6
AD1	V5
AD2	AA8
AD3	AA6
AD4	R6
AD5	W7
AD6	V7
AD7	Y9
AD8	T6
AD9	Y8
AD10	T4
AD11	U6
AD12	T5
AD13	W9
AD14	U7
DQS0_P	Y3
DQS0_N	AA3
DQS1_P	R3
DQS1_N	R2
MEM_DM0	AB2
MEM_DM1	U3
MA0_CKE0	R4

DQS1_N	R3
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