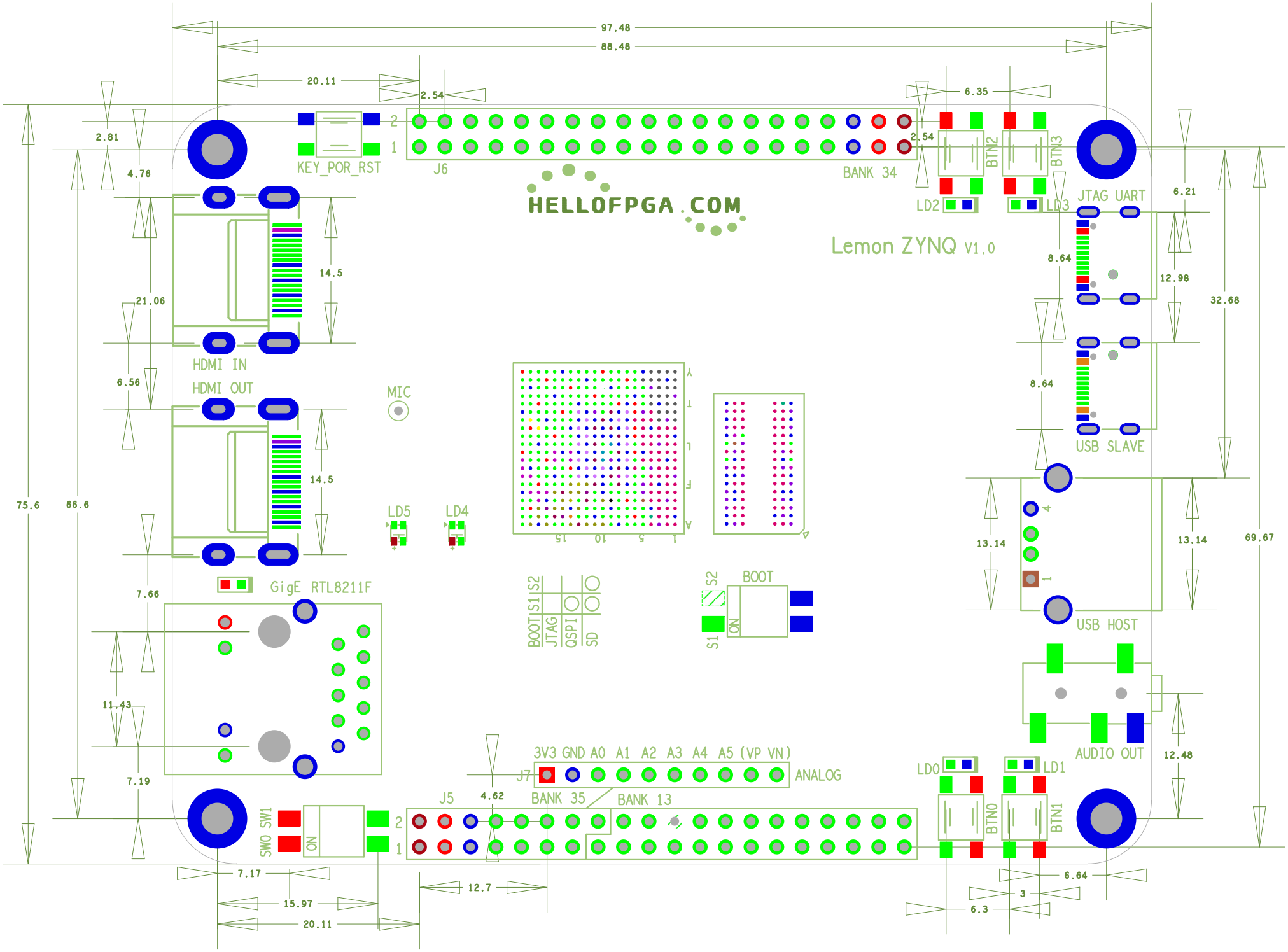
97.48
88.48
20.11
2.54
6.35
2.81
4.76
KEY_POR_RST
J6
BANK 34
BTN2
BTN3
LD2
LD3
HELLOFPGA.COM
Lemon ZYNQ V1.0
JTAG UART
6.21
8.64
12.98
32.68
14.5
21.06
HDMI IN
HDMI OUT
6.56
MIC
USB SLAVE
75.6
66.6
LD5
LD4
13.14
69.67
7.66
GigE RTL8211F
BOOT
S2
S1
ON
USB HOST
11.43
AUDIO OUT
12.48
3V3 GND A0 A1 A2 A3 A4 A5 (VP VN)
J7
ANALOG
LD0
LD1
7.19
J5
4.62
BANK 35
BANK 13
SW1
SW0
BTN0
BTN1
7.17
12.7
6.64
15.97
3
20.11
6.3