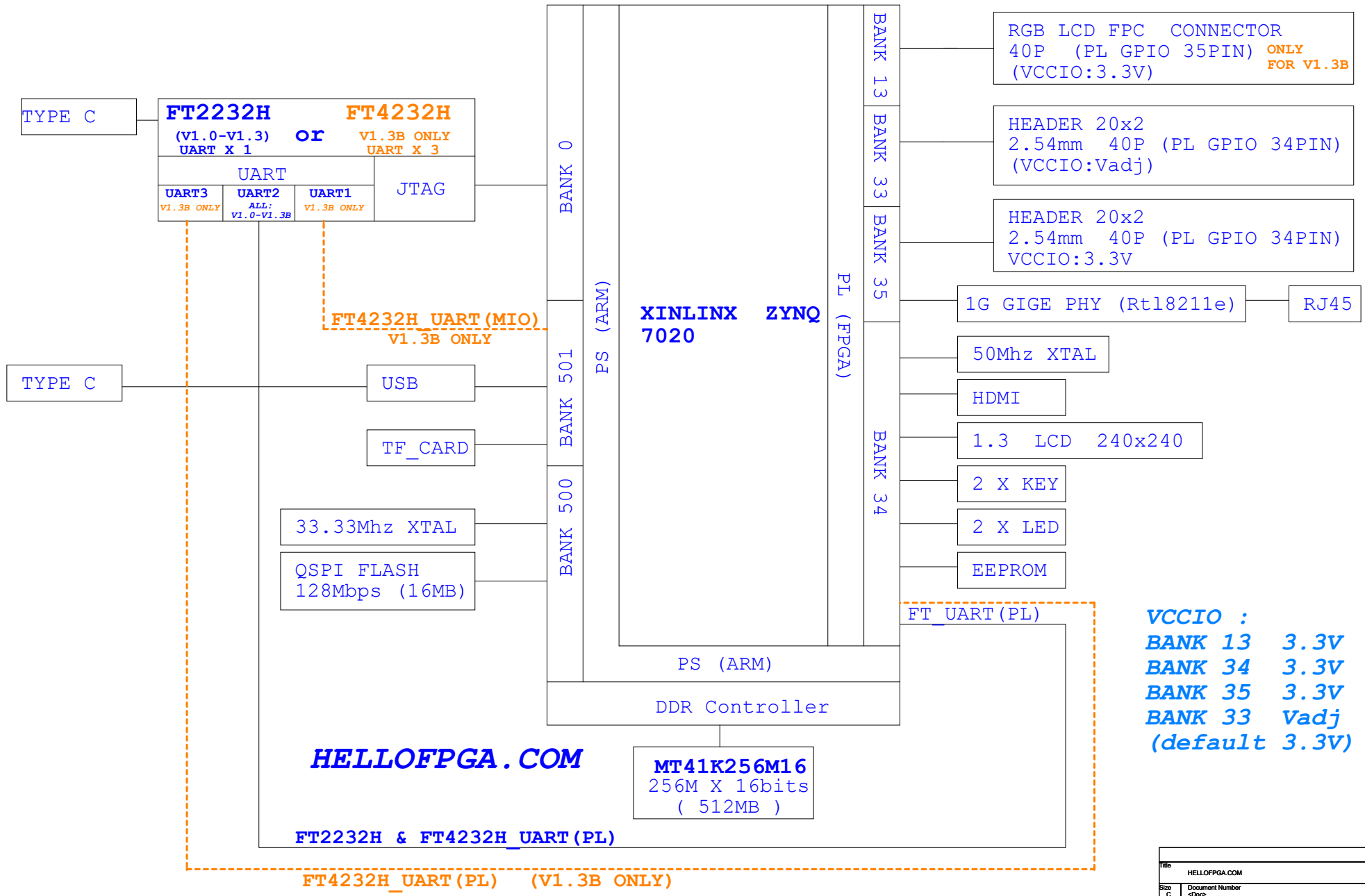
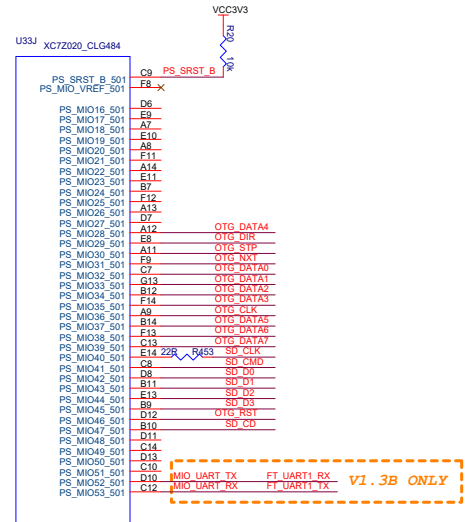
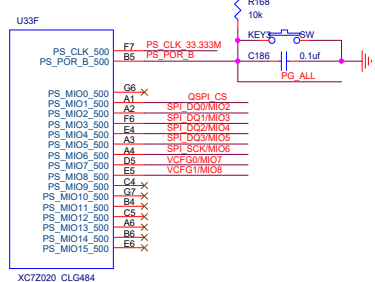
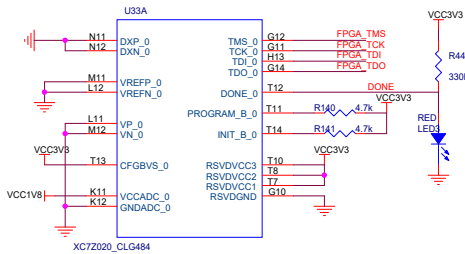


Smart ZYNQ SP2 V1.3/V1.3B Block Diagram

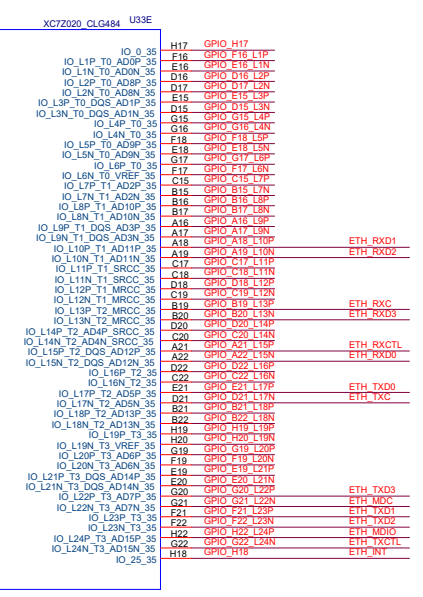
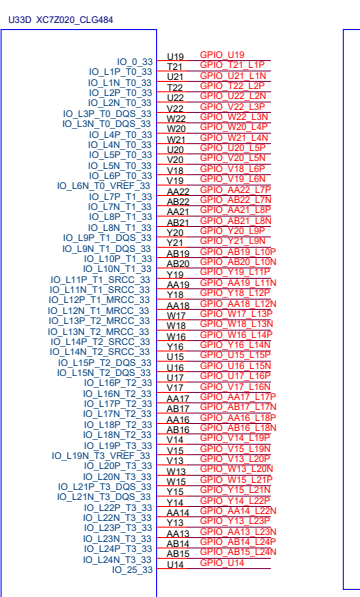
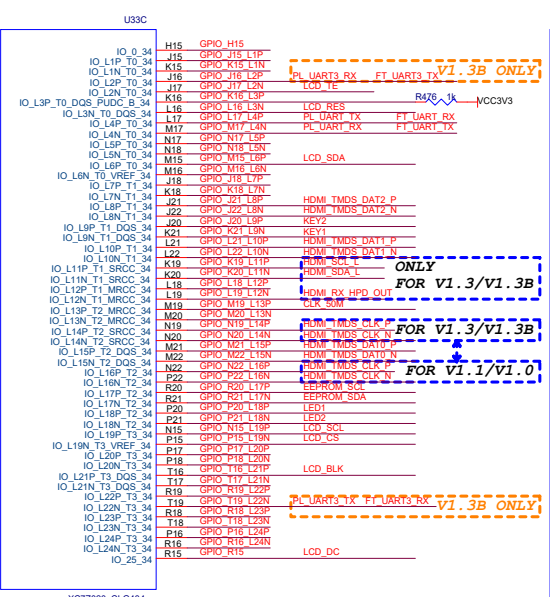
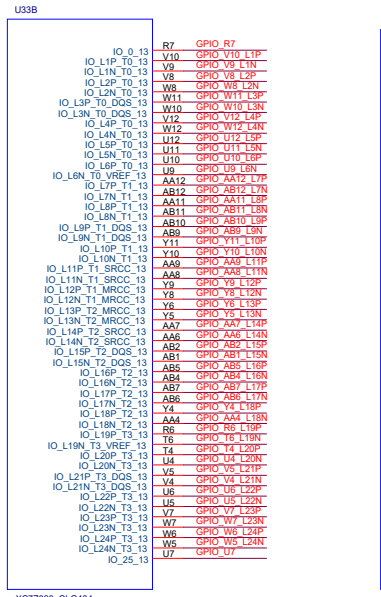
此原理图同样适用于v1.0,v1.1和v1.2版本硬件电路

This schematic is also applicable to the V1.0 V1.1 and V1.2 version hardware circuits.

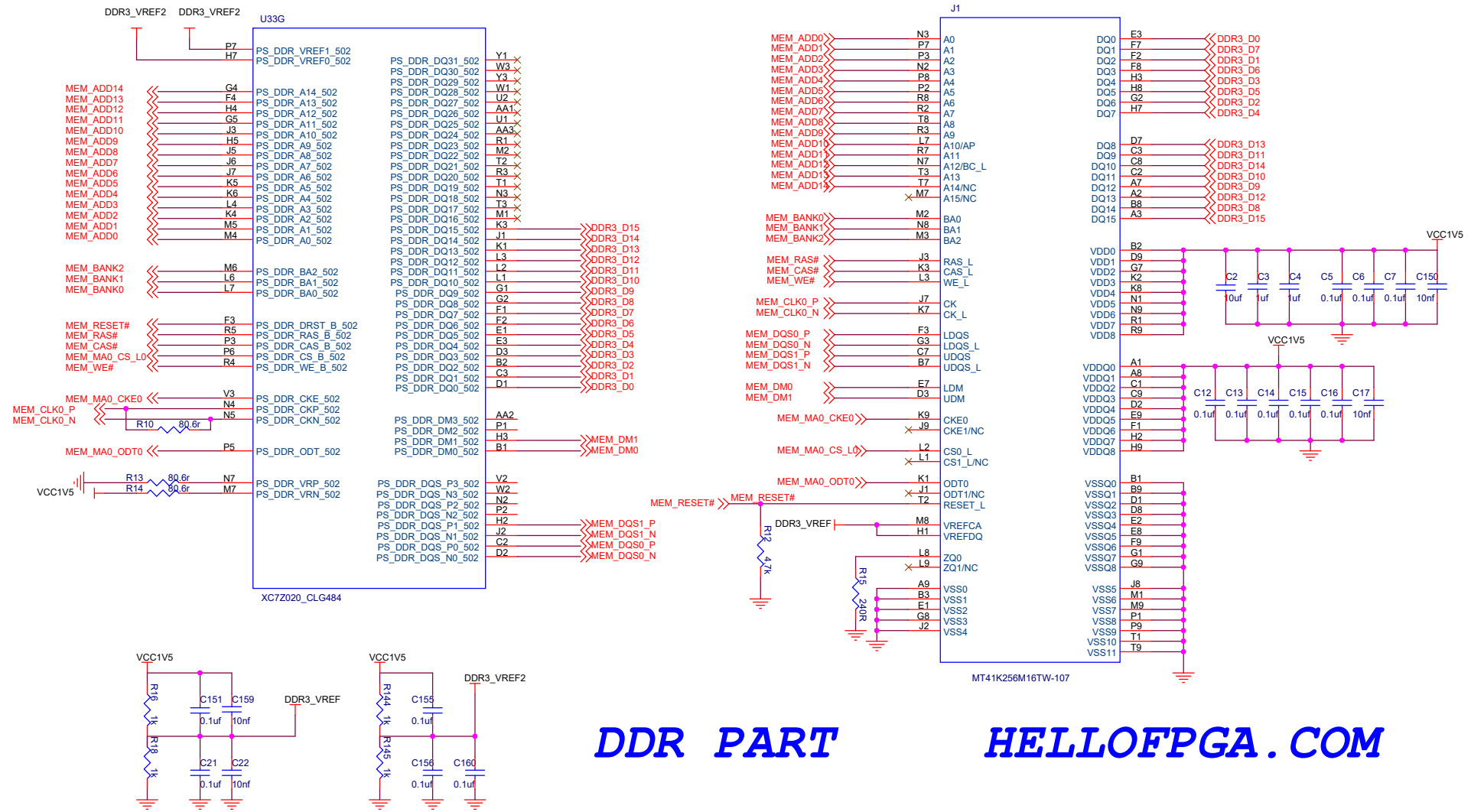




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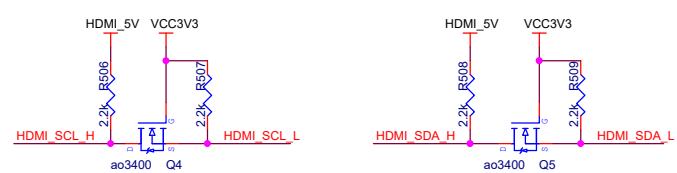
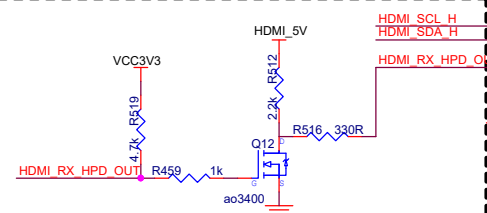
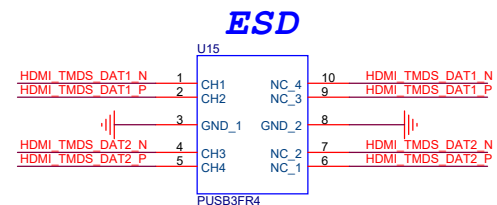
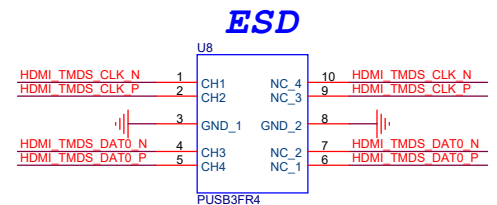
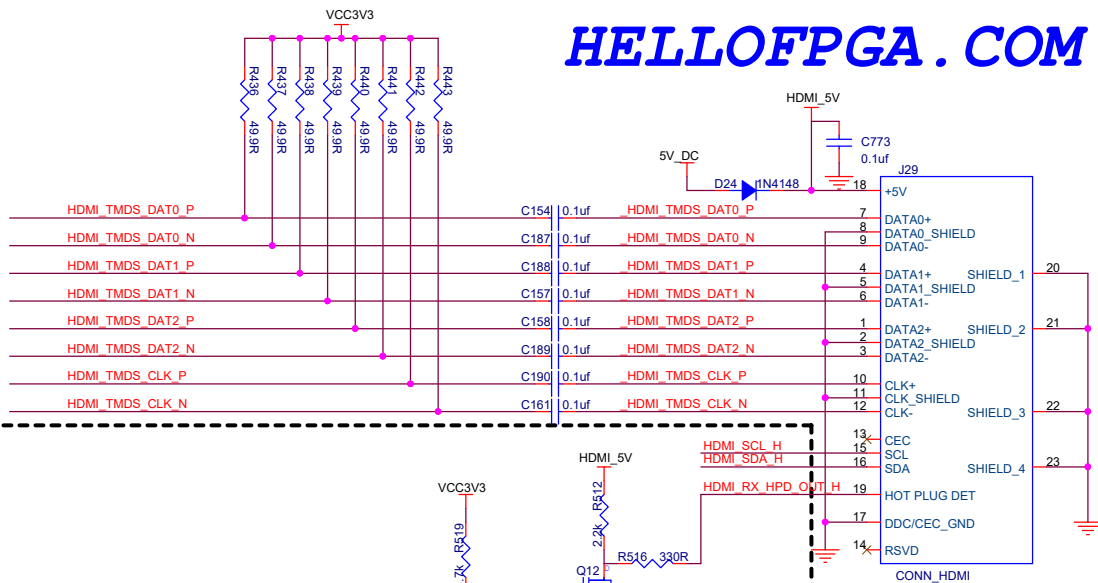


版本信息标注在主板的丝印上
Please check the version information indicated on the silk-screen markings of the motherboard



DDR PART **HELLOFPGA.COM**

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		Rev	V1.3B



HDMI

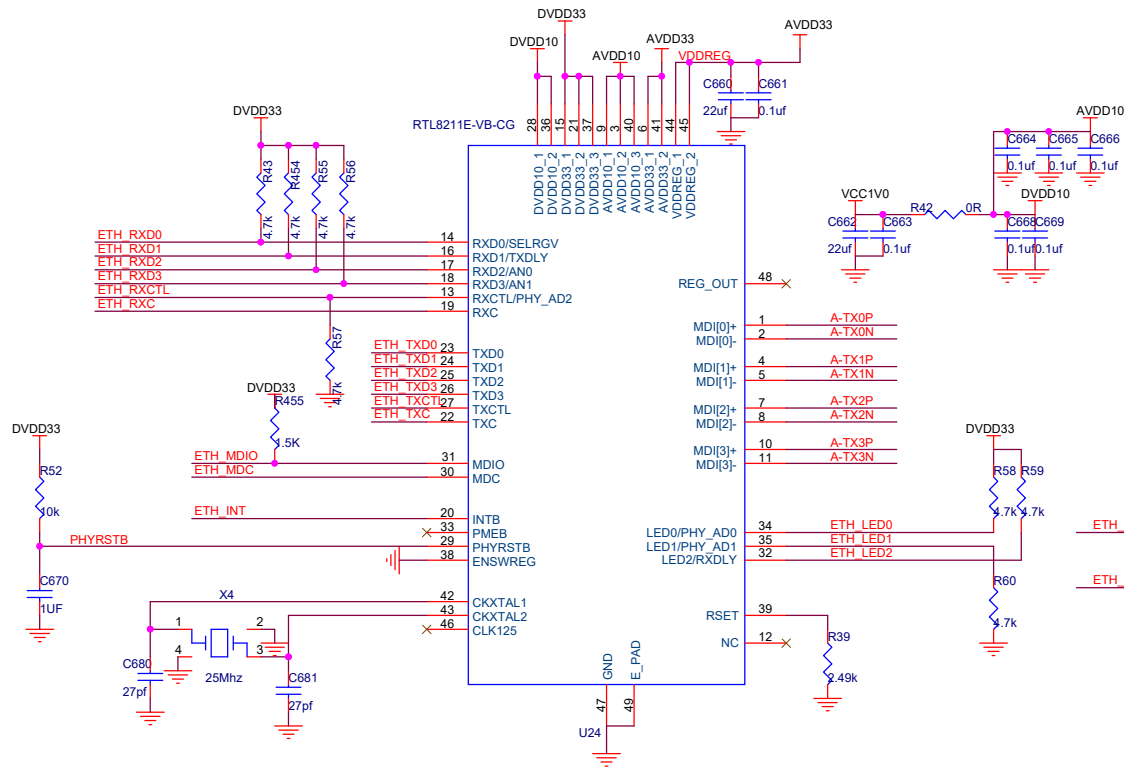
注意: v1.3/v1.3B版本硬件中新增HDMI_SDA, HDMI_SCL, RX_HPD_OUT 三个信号 (v1.1/v1.0中不存在)

Note: The circuit version 1.3/1.3B introduces three new HDMI signals SDA, SCL, and RX_HPD_OUT which are not present in circuit versions 1.1 and 1.0.

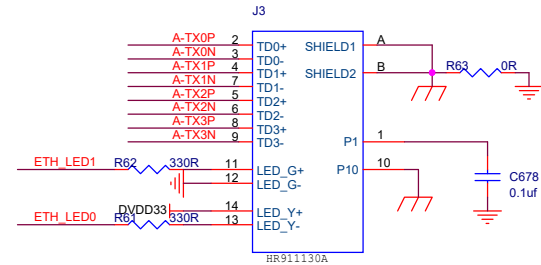
版本信息标注在主板的丝印上

Please check the version information indicated on the silk-screen markings of the motherboard

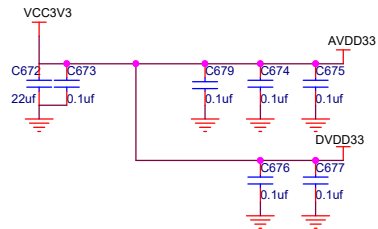
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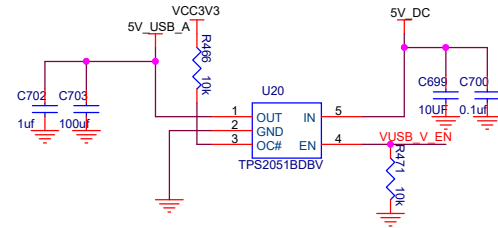
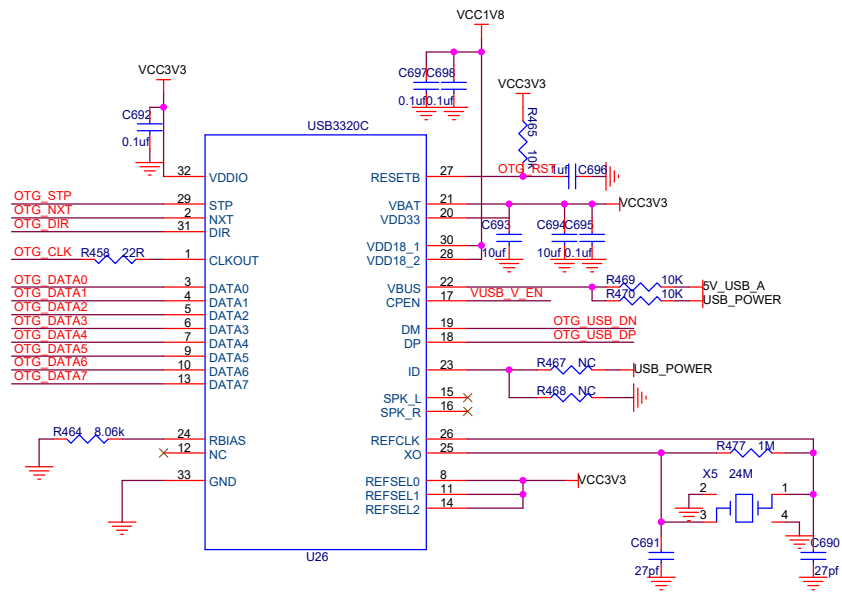
NET PART



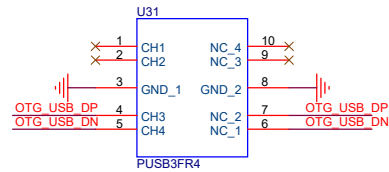
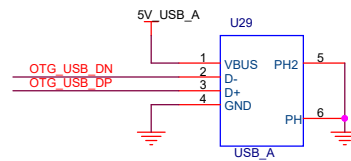
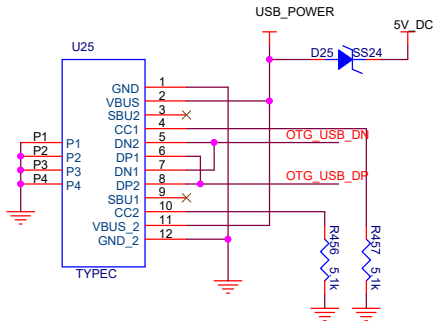
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Size B	Document Number <Doc>	Rev V1.3B
Date:	Tuesday, April 14, 2026	Sheet 1 of 1



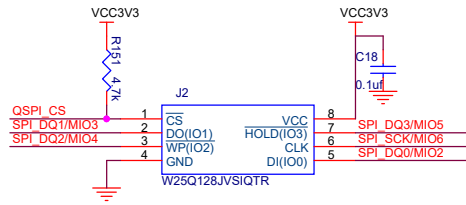
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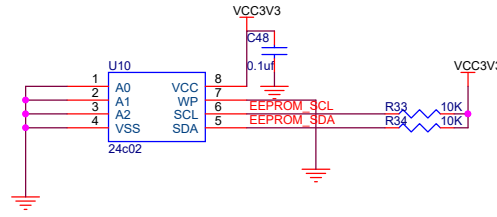
USB PART

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HELLOFPGA.COM		
Size	Document Number	Rev
B	<Doc>	V1.3B
Date:	Tuesday, April 14, 2026	Sheet 1 of 1

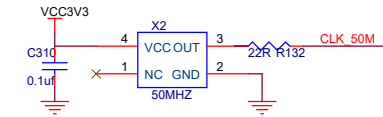
QSPI FLASH



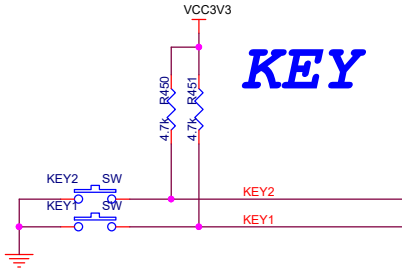
EEPROM



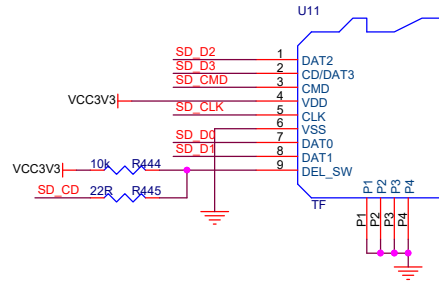
PL CLK



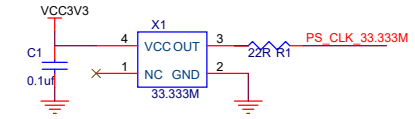
KEY



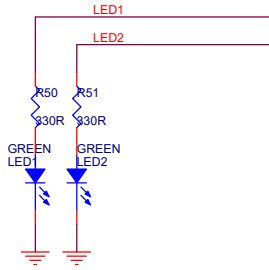
TF CARD



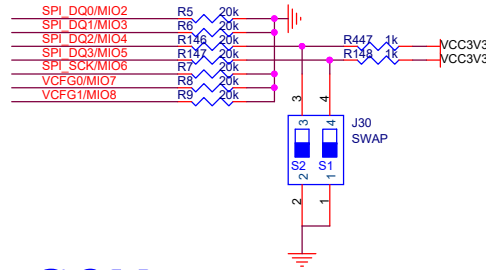
PS CLK



LED



BOOT SELECTION

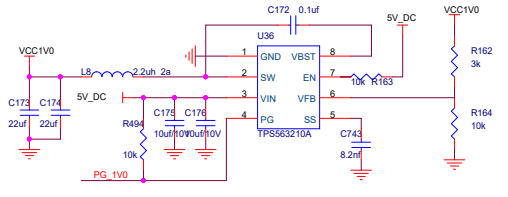
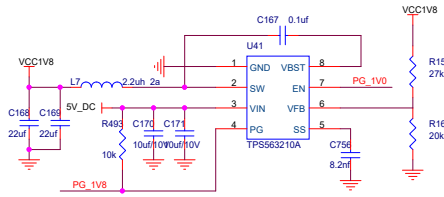
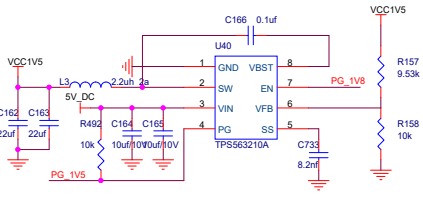


BOOT SELECTION

BOOT	S1	S2
JTAG	●	●
QSPI	○	●
SD	○	○

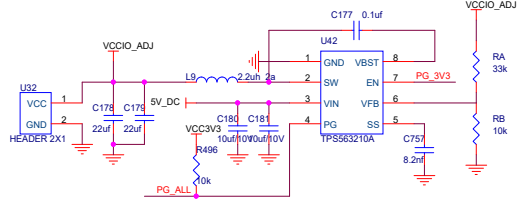
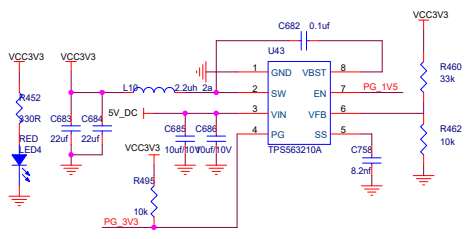
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POWER

VADJ

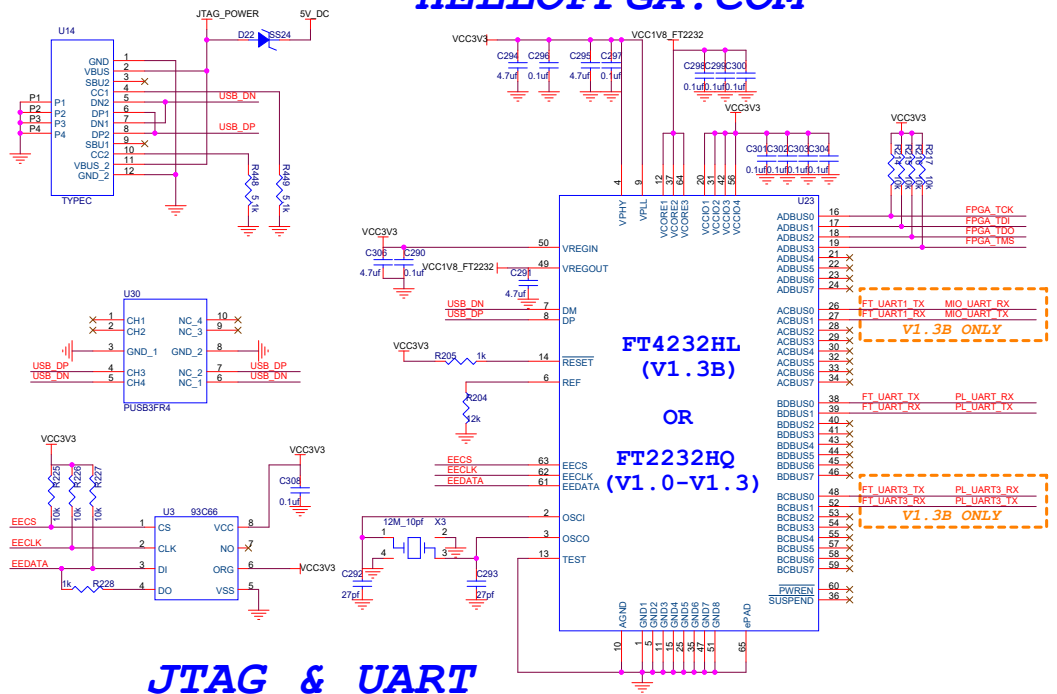


Default Vadj = 3.3V

VADJ	RA	RB
3.3V	33K	10K
2.5V	22.6K	10K
1.8V	13.7K	10K

Default Vadj = 3.3V

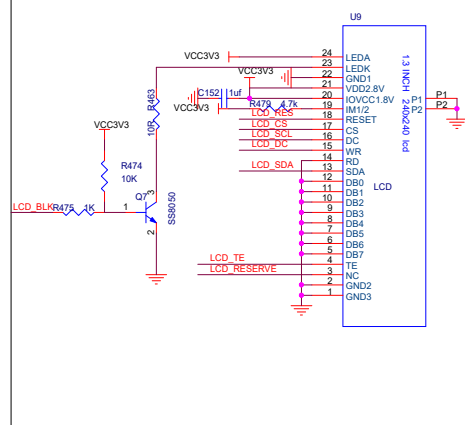
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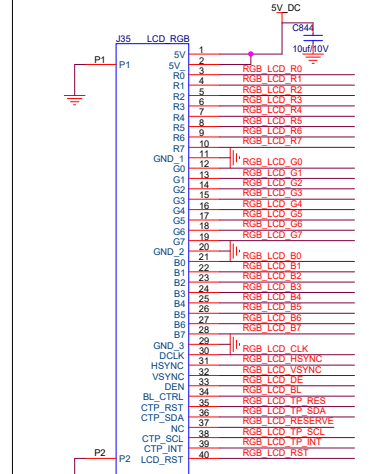
JTAG & UART

FT4232HL 3X UART
FT2232HL 1X UART

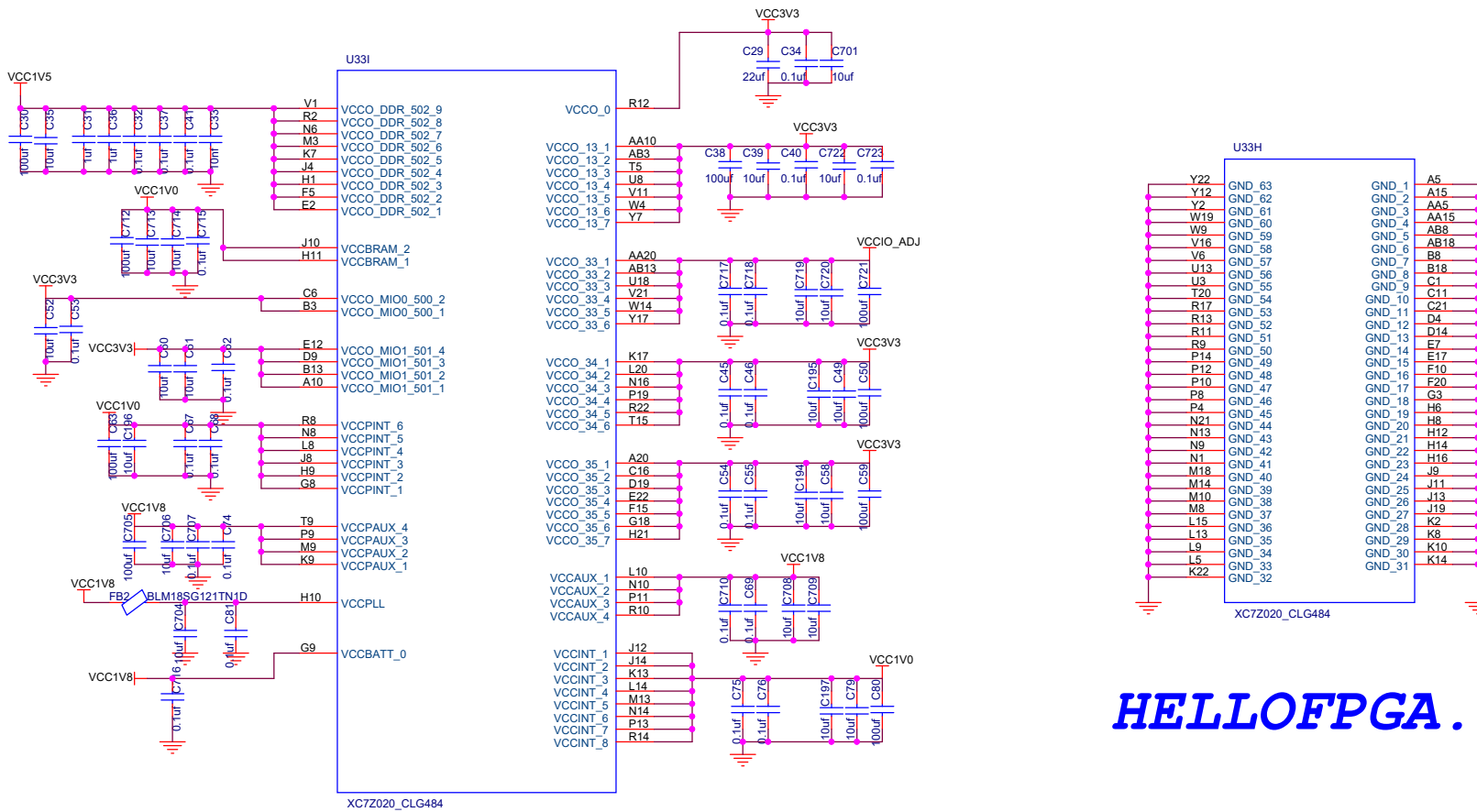
1.3 INCH LCD



RGB LCD



ONLY FOR V1.3B



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UART

ZYNQ_TX	L17
---------	-----

ZYNQ_RX	M17
---------	-----

EEPROM

SCL	R20
-----	-----

SDA	R21
-----	-----

50M CLOCK

CLK	M19
-----	-----

HDMI

V1.0/V1.1 V1.3/V1.3B

CLK	N22	N19
-----	-----	-----

D0	M21	M21
----	-----	-----

D1	L21	L21
----	-----	-----

D2	J21	J21
----	-----	-----

SDA	/	K20
-----	---	-----

SCL	/	K19
-----	---	-----

RX_HP_D_OUT	/	L19
-------------	---	-----

KEY & LED

KEY1	K21
------	-----

KEY2	J20
------	-----

LED1	P20
------	-----

LED2	P21
------	-----

LCD 240x240

LCD_DC	R15
--------	-----

LCD_CS	P15
--------	-----

LCD_SCL	N15
---------	-----

LCD_SDA	M15
---------	-----

LCD_RES	L16
---------	-----

LCD_BLK	T16
---------	-----

LCD_TE	J17
--------	-----

(LCD BLK:default high level by
External pull-up resistance)

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GigE phy

ETH_TD0	E21
---------	-----

ETH_TD1	F21
---------	-----

ETH_TD2	F22
---------	-----

ETH_TD3	G20
---------	-----

ETH_TX_CTL	G22
------------	-----

ETH_TXC	D21
---------	-----

ETH_RD0	A22
---------	-----

ETH_RD1	A18
---------	-----

ETH_RD2	A19
---------	-----

ETH_RD3	B20
---------	-----

ETH_RX_CTL	A21
------------	-----

ETH_RXC	B19
---------	-----

ETH_MDIO	H22
----------	-----

ETH_MDC	G21
---------	-----

ETH_INT	H18
---------	-----

RGB_LCD

R7	Y4
----	----

R6	V10
----	-----

R5	AB12
----	------

R4	U10
----	-----

R3	AA8
----	-----

R2	AB7
----	-----

R1	AA12
----	------

R0	V7
----	----

G7	AB10
----	------

G6	AA9
----	-----

G5	Y9
----	----

G4	W8
----	----

G3	Y8
----	----

G2	Y6
----	----

G1	V8
----	----

G0	AB9
----	-----

B7	W6
----	----

B6	AB5
----	-----

B5	AB4
----	-----

B4	AB6
----	-----

B3	W7
----	----

B2	AA7
----	-----

B1	V4
----	----

B0	Y5
----	----

HSYNC	V9
-------	----

VSYNC	AB2
-------	-----

CLK	AA4
-----	-----

DE	AA6
----	-----

BL	U7
----	----

RST (RESERVE)	W5
---------------	----

TP_RES	U6
--------	----

TP_INT	U4
--------	----

TP_SCL	U5
--------	----

TP_SDA	AB1
--------	-----

TOUCH

(RESERVE)	V5
-----------	----

Smart ZYNQ SP2 board Pin Constraint Definition Reference

```

create_clock -period 20 -name clk_50 [get_ports clk_50]
set_property -dict {PACKAGE_PIN M19 IOSTANDARD LVCMOS33} [get_ports clk_50]

set_property -dict {PACKAGE_PIN M17 IOSTANDARD LVCMOS33} [get_ports uart_rxd]
set_property -dict {PACKAGE_PIN M17 IOSTANDARD LVCMOS33} [get_ports uart_txd]
set_property -dict {PACKAGE_PIN J16 IOSTANDARD LVCMOS33} [get_ports uart_rxd]
set_property -dict {PACKAGE_PIN J19 IOSTANDARD LVCMOS33} [get_ports uart_txd]
##### ONLY FOR V1.3B #####

set_property -dict {PACKAGE_PIN P20 IOSTANDARD LVCMOS33} [get_ports LED1]
set_property -dict {PACKAGE_PIN K21 IOSTANDARD LVCMOS33} [get_ports LED2]
set_property -dict {PACKAGE_PIN K21 IOSTANDARD LVCMOS33} [get_ports KEY1]
set_property -dict {PACKAGE_PIN J20 IOSTANDARD LVCMOS33} [get_ports KEY2]

set_property -dict {PACKAGE_PIN P20 IOSTANDARD LVCMOS33} [get_ports EEPROM_SCL]
set_property -dict {PACKAGE_PIN R21 IOSTANDARD LVCMOS33} [get_ports EEPROM_SDA]

# RGMII PHY
create_clock -period 8 -name RGMII_tx [get_ports RGMII_tx]
set_property -dict {PACKAGE_PIN G21 IOSTANDARD LVCMOS33} [get_ports MDIO_PHY_mdio]
set_property -dict {PACKAGE_PIN H22 IOSTANDARD LVCMOS33} [get_ports MDIO_PHY_mdio_io]
set_property -dict {PACKAGE_PIN A22 IOSTANDARD LVCMOS33} [get_ports {RGMII_rd[0]}]
set_property -dict {PACKAGE_PIN A18 IOSTANDARD LVCMOS33} [get_ports {RGMII_rd[1]}]
set_property -dict {PACKAGE_PIN A19 IOSTANDARD LVCMOS33} [get_ports {RGMII_rd[2]}]
set_property -dict {PACKAGE_PIN B20 IOSTANDARD LVCMOS33} [get_ports {RGMII_rd[3]}]
set_property -dict {PACKAGE_PIN A21 IOSTANDARD LVCMOS33} [get_ports {RGMII_rx_ctl1}]
set_property -dict {PACKAGE_PIN B19 IOSTANDARD LVCMOS33} [get_ports {RGMII_rxc}]
set_property -dict {PACKAGE_PIN E21 IOSTANDARD LVCMOS33} [get_ports {RGMII_td[0]}]
set_property -dict {PACKAGE_PIN F21 IOSTANDARD LVCMOS33} [get_ports {RGMII_td[1]}]
set_property -dict {PACKAGE_PIN F22 IOSTANDARD LVCMOS33} [get_ports {RGMII_td[2]}]
set_property -dict {PACKAGE_PIN G20 IOSTANDARD LVCMOS33} [get_ports {RGMII_td[3]}]
set_property -dict {PACKAGE_PIN G22 IOSTANDARD LVCMOS33} [get_ports {RGMII_tx_ctl1}]
set_property -dict {PACKAGE_PIN D21 IOSTANDARD LVCMOS33} [get_ports {RGMII_tx}]
set_property SLEW_FAST [get_ports {RGMII_td[0]}]
set_property SLEW_FAST [get_ports {RGMII_td[1]}]
set_property SLEW_FAST [get_ports {RGMII_td[2]}]
set_property SLEW_FAST [get_ports {RGMII_td[3]}]
set_property SLEW_FAST [get_ports {RGMII_tx_ctl1}]
set_property SLEW_FAST [get_ports {RGMII_tx}]
##### ONLY FOR V1.3B #####

```

V1.0/V1.1

```

# VER_V1.0 / V1.1
# HDMI (DVI) outputs
set_property PACKAGE_PIN J21 [get_ports {hdmi_d_p[2]}]
set_property PACKAGE_PIN L21 [get_ports {hdmi_d_p[1]}]
set_property PACKAGE_PIN M21 [get_ports {hdmi_d_p[0]}]
set_property PACKAGE_PIN N22 [get_ports {hdmi_clk_p}]

# VER_V1.3 / V1.3B
# HDMI (DVI) outputs
set_property PACKAGE_PIN J21 [get_ports {hdmi_d_p[2]}]
set_property PACKAGE_PIN L21 [get_ports {hdmi_d_p[1]}]
set_property PACKAGE_PIN M21 [get_ports {hdmi_d_p[0]}]

set_property PACKAGE_PIN N19 [get_ports {hdmi_clk_p}]
set_property -dict {PACKAGE_PIN K20 IOSTANDARD LVCMOS33} [get_ports {HDMI_SDA}]
set_property -dict {PACKAGE_PIN K19 IOSTANDARD LVCMOS33} [get_ports {HDMI_SCL}]
set_property -dict {PACKAGE_PIN L19 IOSTANDARD LVCMOS33} [get_ports {HDMI_RX_HP}]

```

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```

## J5 on board (BANK35 V3V3)
# Set voltage level for banks35 (match with jumper setting on board)
set_property IOSTANDARD LVCMOS33 [get_ports {J5[*]}]
set_property PACKAGE_PIN H19 [get_ports {J5[0]}]; #IO B35 LP19
set_property PACKAGE_PIN H20 [get_ports {J5[1]}]; #IO B35 LN19
set_property PACKAGE_PIN E18 [get_ports {J5[2]}]; #IO B35 LN5
set_property PACKAGE_PIN F18 [get_ports {J5[3]}]; #IO B35 LP5
set_property PACKAGE_PIN G17 [get_ports {J5[4]}]; #IO B35 LN6
set_property PACKAGE_PIN G17 [get_ports {J5[5]}]; #IO B35 LP6
set_property PACKAGE_PIN C17 [get_ports {J5[6]}]; #IO B35 LP11
set_property PACKAGE_PIN C18 [get_ports {J5[7]}]; #IO B35 LN11
set_property PACKAGE_PIN E19 [get_ports {J5[8]}]; #IO B35 LP20
set_property PACKAGE_PIN F19 [get_ports {J5[9]}]; #IO B35 LN20
set_property PACKAGE_PIN G20 [get_ports {J5[10]}]; #IO B35 LN21
set_property PACKAGE_PIN E19 [get_ports {J5[11]}]; #IO B35 LP21
set_property PACKAGE_PIN D22 [get_ports {J5[12]}]; #IO B35 LP16
set_property PACKAGE_PIN C22 [get_ports {J5[13]}]; #IO B35 LN16
set_property PACKAGE_PIN B22 [get_ports {J5[14]}]; #IO B35 LN18
set_property PACKAGE_PIN B21 [get_ports {J5[15]}]; #IO B35 LP18
set_property PACKAGE_PIN B17 [get_ports {J5[16]}]; #IO B35 LN8
set_property PACKAGE_PIN B16 [get_ports {J5[17]}]; #IO B35 LP8
set_property PACKAGE_PIN A17 [get_ports {J5[18]}]; #IO B35 LN9
set_property PACKAGE_PIN A16 [get_ports {J5[19]}]; #IO B35 LP9
set_property PACKAGE_PIN D20 [get_ports {J5[20]}]; #IO B35 LP14
set_property PACKAGE_PIN C20 [get_ports {J5[21]}]; #IO B35 LN14
set_property PACKAGE_PIN C15 [get_ports {J5[22]}]; #IO B35 LP7
set_property PACKAGE_PIN C15 [get_ports {J5[23]}]; #IO B35 LN7
set_property PACKAGE_PIN D17 [get_ports {J5[24]}]; #IO B35 LN2
set_property PACKAGE_PIN D16 [get_ports {J5[25]}]; #IO B35 LP2
set_property PACKAGE_PIN E15 [get_ports {J5[26]}]; #IO B35 LN3
set_property PACKAGE_PIN E15 [get_ports {J5[27]}]; #IO B35 LP3
set_property PACKAGE_PIN D18 [get_ports {J5[28]}]; #IO B35 LP12
set_property PACKAGE_PIN C19 [get_ports {J5[29]}]; #IO B35 LN12
set_property PACKAGE_PIN E16 [get_ports {J5[30]}]; #IO B35 LN1
set_property PACKAGE_PIN F16 [get_ports {J5[31]}]; #IO B35 LP1
set_property PACKAGE_PIN G15 [get_ports {J5[32]}]; #IO B35 LP4
set_property PACKAGE_PIN G16 [get_ports {J5[33]}]; #IO B35 LN4

## J6 on board (BANK33 VADJ)
# Set voltage level for banks 33 (match with jumper setting on board)
set_property IOSTANDARD LVCMOS33 [get_ports {J6[*]}]
set_property PACKAGE_PIN U22 [get_ports {J6[0]}]; #J6/1 = IO B33 LN2
set_property PACKAGE_PIN T22 [get_ports {J6[1]}]; #J6/2 = IO B33 LP2
set_property PACKAGE_PIN W22 [get_ports {J6[2]}]; #J6/3 = IO B33 LN3
set_property PACKAGE_PIN V22 [get_ports {J6[3]}]; #J6/4 = IO B33 LP3
set_property PACKAGE_PIN Y21 [get_ports {J6[4]}]; #J6/5 = IO B33 LN9
set_property PACKAGE_PIN Y20 [get_ports {J6[5]}]; #J6/6 = IO B33 LP9
set_property PACKAGE_PIN AB22 [get_ports {J6[6]}]; #J6/7 = IO B33 LN7
set_property PACKAGE_PIN AA22 [get_ports {J6[7]}]; #J6/8 = IO B33 LP7
set_property PACKAGE_PIN AB21 [get_ports {J6[8]}]; #J6/9 = IO B33 LN8
set_property PACKAGE_PIN AA21 [get_ports {J6[9]}]; #J6/10 = IO B33 LP8
set_property PACKAGE_PIN AB19 [get_ports {J6[10]}]; #J6/11 = IO B33 LP10
set_property PACKAGE_PIN AB20 [get_ports {J6[11]}]; #J6/12 = IO B33 LN10
set_property PACKAGE_PIN AA19 [get_ports {J6[12]}]; #J6/13 = IO B33 LN11
set_property PACKAGE_PIN Y19 [get_ports {J6[13]}]; #J6/14 = IO B33 LP11
set_property PACKAGE_PIN Y18 [get_ports {J6[14]}]; #J6/15 = IO B33 LN18
set_property PACKAGE_PIN AA16 [get_ports {J6[15]}]; #J6/16 = IO B33 LP18
set_property PACKAGE_PIN Y18 [get_ports {J6[16]}]; #J6/17 = IO B33 LP12
set_property PACKAGE_PIN AA18 [get_ports {J6[17]}]; #J6/18 = IO B33 LN12
set_property PACKAGE_PIN AB14 [get_ports {J6[18]}]; #J6/19 = IO B33 LP24
set_property PACKAGE_PIN AB15 [get_ports {J6[19]}]; #J6/20 = IO B33 LN24
set_property PACKAGE_PIN Y13 [get_ports {J6[20]}]; #J6/21 = IO B33 LP23
set_property PACKAGE_PIN AA13 [get_ports {J6[21]}]; #J6/22 = IO B33 LN23
set_property PACKAGE_PIN Y13 [get_ports {J6[22]}]; #J6/23 = IO B33 LP20
set_property PACKAGE_PIN W13 [get_ports {J6[23]}]; #J6/24 = IO B33 LN20
set_property PACKAGE_PIN W18 [get_ports {J6[24]}]; #J6/25 = IO B33 LN13
set_property PACKAGE_PIN W17 [get_ports {J6[25]}]; #J6/26 = IO B33 LP13
set_property PACKAGE_PIN AA17 [get_ports {J6[26]}]; #J6/27 = IO B33 LP17
set_property PACKAGE_PIN AB17 [get_ports {J6[27]}]; #J6/28 = IO B33 LN17
set_property PACKAGE_PIN W16 [get_ports {J6[28]}]; #J6/29 = IO B33 LP14
set_property PACKAGE_PIN Y14 [get_ports {J6[29]}]; #J6/30 = IO B33 LN14
set_property PACKAGE_PIN Y14 [get_ports {J6[30]}]; #J6/31 = IO B33 LP22
set_property PACKAGE_PIN AA14 [get_ports {J6[31]}]; #J6/32 = IO B33 LN22
set_property PACKAGE_PIN W15 [get_ports {J6[32]}]; #J6/33 = IO B33 LN19
set_property PACKAGE_PIN V14 [get_ports {J6[33]}]; #J6/34 = IO B33 LP19

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##### R #####
set_property -dict {PACKAGE_PIN V4 IOSTANDARD LVCMOS33} [get_ports {RGB_LCD_R[7]}]
set_property -dict {PACKAGE_PIN V10 IOSTANDARD LVCMOS33} [get_ports {RGB_LCD_R[6]}]
set_property -dict {PACKAGE_PIN AB12 IOSTANDARD LVCMOS33} [get_ports {RGB_LCD_R[5]}]
set_property -dict {PACKAGE_PIN U10 IOSTANDARD LVCMOS33} [get_ports {RGB_LCD_R[4]}]
set_property -dict {PACKAGE_PIN AA8 IOSTANDARD LVCMOS33} [get_ports {RGB_LCD_R[3]}]
set_property -dict {PACKAGE_PIN AB7 IOSTANDARD LVCMOS33} [get_ports {RGB_LCD_R[2]}]
set_property -dict {PACKAGE_PIN AA12 IOSTANDARD LVCMOS33} [get_ports {RGB_LCD_R[1]}]
set_property -dict {PACKAGE_PIN V7 IOSTANDARD LVCMOS33} [get_ports {RGB_LCD_R[0]}]
##### G #####
set_property -dict {PACKAGE_PIN AB10 IOSTANDARD LVCMOS33} [get_ports {RGB_LCD_G[7]}]
set_property -dict {PACKAGE_PIN AA9 IOSTANDARD LVCMOS33} [get_ports {RGB_LCD_G[6]}]
set_property -dict {PACKAGE_PIN V9 IOSTANDARD LVCMOS33} [get_ports {RGB_LCD_G[5]}]
set_property -dict {PACKAGE_PIN W8 IOSTANDARD LVCMOS33} [get_ports {RGB_LCD_G[4]}]
set_property -dict {PACKAGE_PIN V8 IOSTANDARD LVCMOS33} [get_ports {RGB_LCD_G[3]}]
set_property -dict {PACKAGE_PIN Y6 IOSTANDARD LVCMOS33} [get_ports {RGB_LCD_G[2]}]
set_property -dict {PACKAGE_PIN V8 IOSTANDARD LVCMOS33} [get_ports {RGB_LCD_G[1]}]
set_property -dict {PACKAGE_PIN AB9 IOSTANDARD LVCMOS33} [get_ports {RGB_LCD_G[0]}]
##### B #####
set_property -dict {PACKAGE_PIN W6 IOSTANDARD LVCMOS33} [get_ports {RGB_LCD_B[7]}]
set_property -dict {PACKAGE_PIN AB5 IOSTANDARD LVCMOS33} [get_ports {RGB_LCD_B[6]}]
set_property -dict {PACKAGE_PIN AB4 IOSTANDARD LVCMOS33} [get_ports {RGB_LCD_B[5]}]
set_property -dict {PACKAGE_PIN AB6 IOSTANDARD LVCMOS33} [get_ports {RGB_LCD_B[4]}]
set_property -dict {PACKAGE_PIN W7 IOSTANDARD LVCMOS33} [get_ports {RGB_LCD_B[3]}]
set_property -dict {PACKAGE_PIN AA7 IOSTANDARD LVCMOS33} [get_ports {RGB_LCD_B[2]}]
set_property -dict {PACKAGE_PIN V4 IOSTANDARD LVCMOS33} [get_ports {RGB_LCD_B[1]}]
set_property -dict {PACKAGE_PIN V5 IOSTANDARD LVCMOS33} [get_ports {RGB_LCD_B[0]}]

##### CONTROL #####
set_property -dict {PACKAGE_PIN V9 IOSTANDARD LVCMOS33} [get_ports {RGB_LCD_HSNC}]
set_property -dict {PACKAGE_PIN AB2 IOSTANDARD LVCMOS33} [get_ports {RGB_LCD_VSNC}]
set_property -dict {PACKAGE_PIN AA4 IOSTANDARD LVCMOS33} [get_ports {RGB_LCD_CLK}]
set_property -dict {PACKAGE_PIN AA6 IOSTANDARD LVCMOS33} [get_ports {RGB_LCD_DE}]

##### BACKLIGHT #####
set_property -dict {PACKAGE_PIN U7 IOSTANDARD LVCMOS33} [get_ports {RGB_LCD_BL}]

##### RST RESERVE #####
set_property -dict {PACKAGE_PIN W5 IOSTANDARD LVCMOS33} [get_ports {RGB_LCD_RST}]

##### TOUCH (I2C) #####
set_property -dict {PACKAGE_PIN U6 IOSTANDARD LVCMOS33} [get_ports {RGB_LCD_TP_RES}]
set_property -dict {PACKAGE_PIN U4 IOSTANDARD LVCMOS33} [get_ports {RGB_LCD_TP_INT}]
set_property -dict {PACKAGE_PIN U5 IOSTANDARD LVCMOS33} [get_ports {RGB_LCD_TP_SCL}]
set_property -dict {PACKAGE_PIN AB1 IOSTANDARD LVCMOS33} [get_ports {RGB_LCD_TP_SDA}]

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RGB LCD FPC CONNECTOR
ONLY FOR V1.3B

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