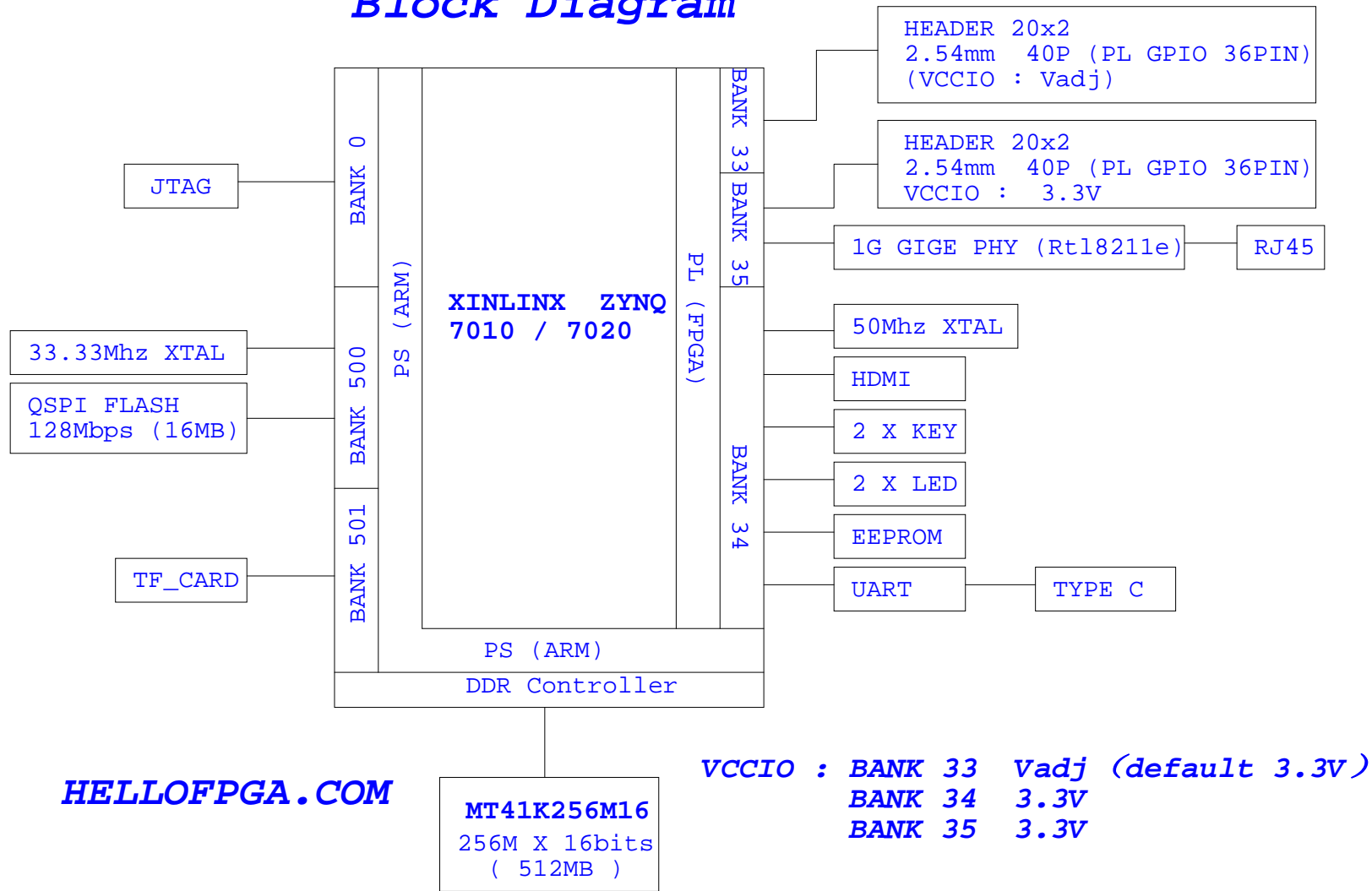
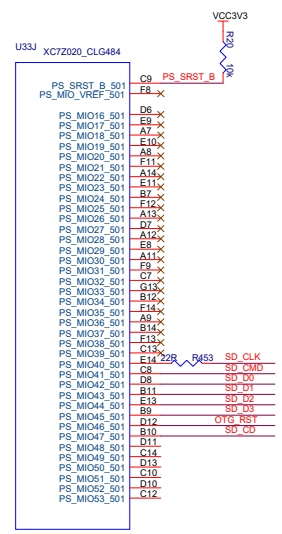
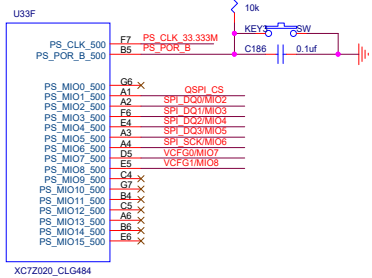
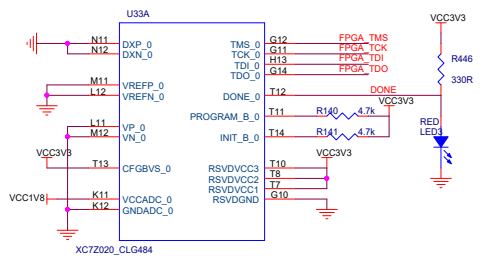
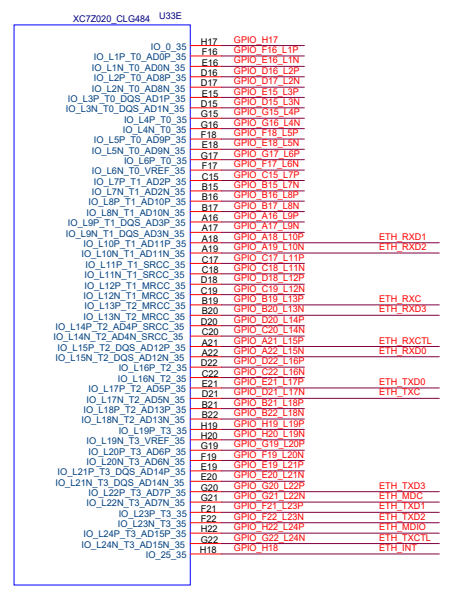
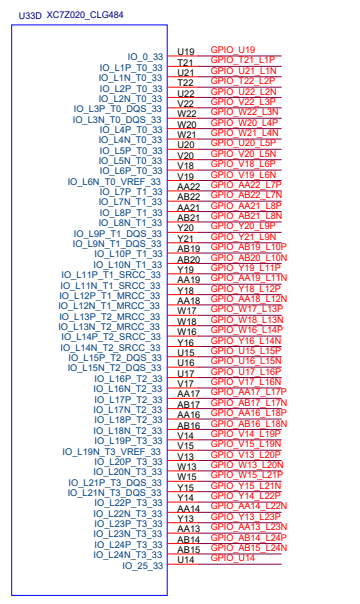
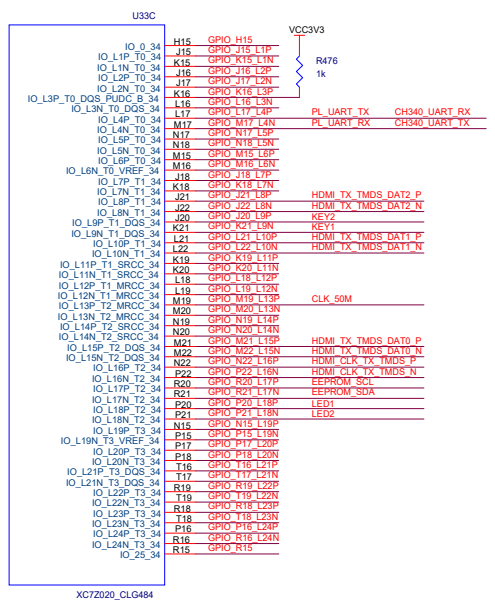
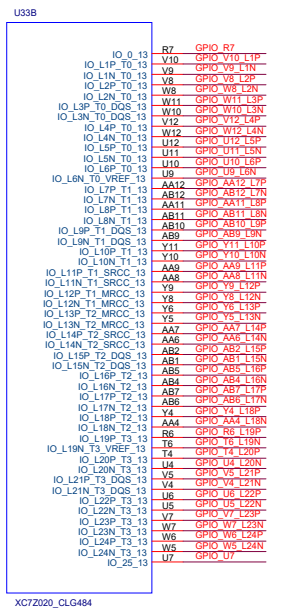


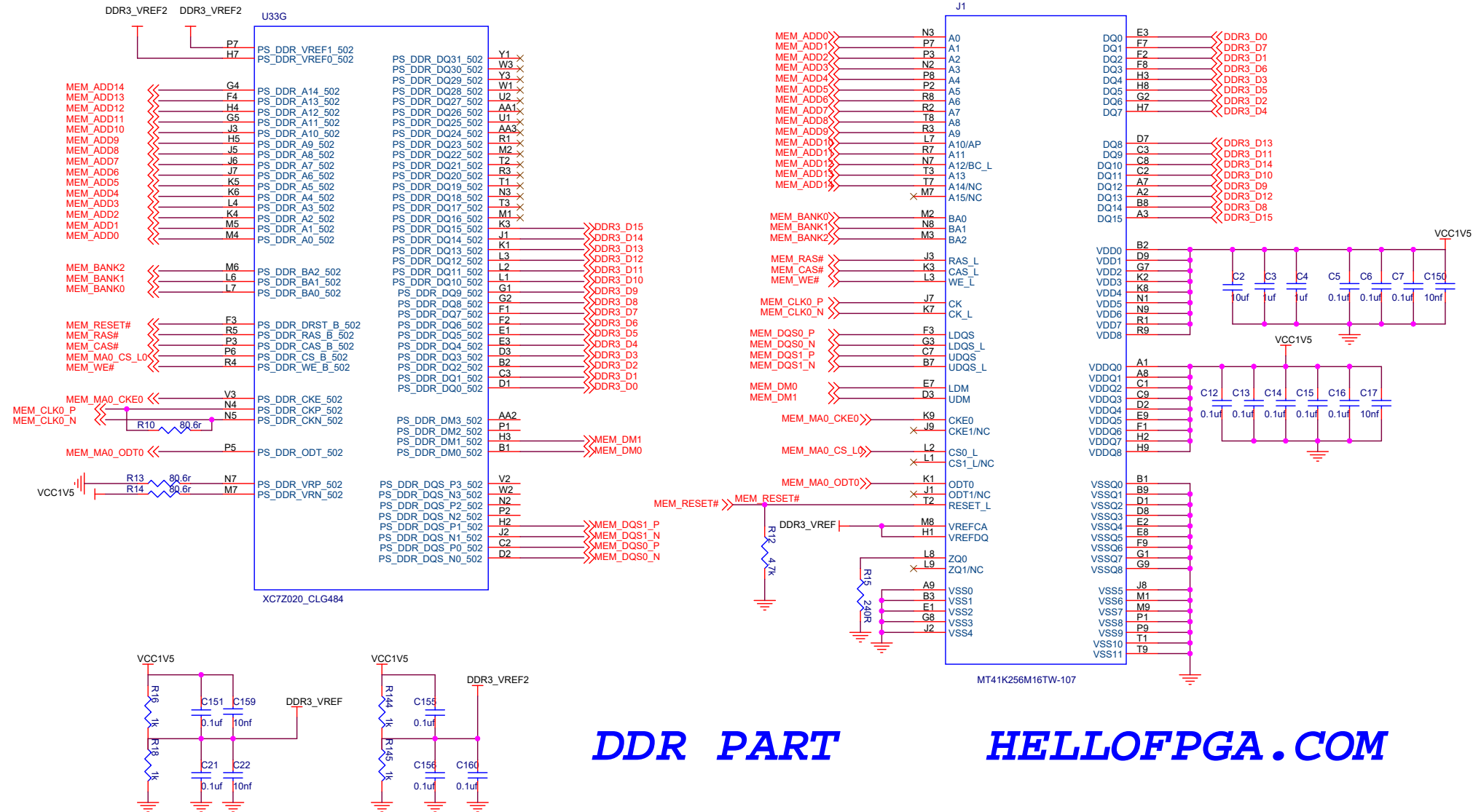
Smart ZYNQ SL Block Diagram





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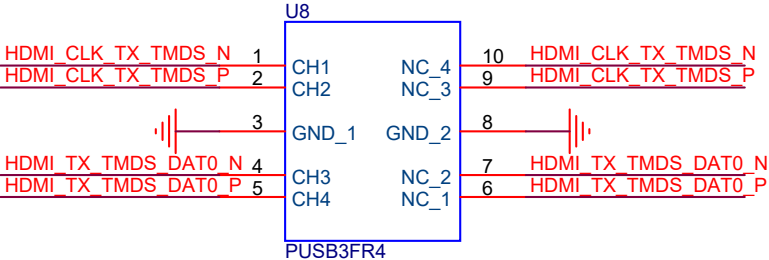
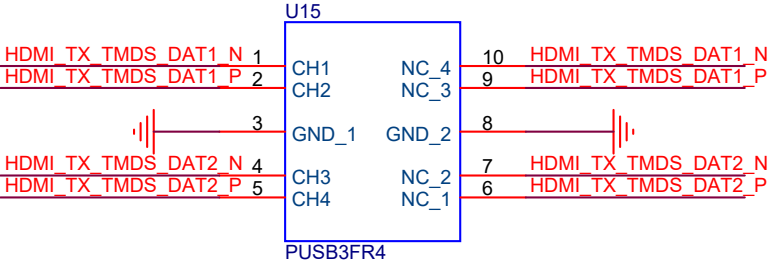
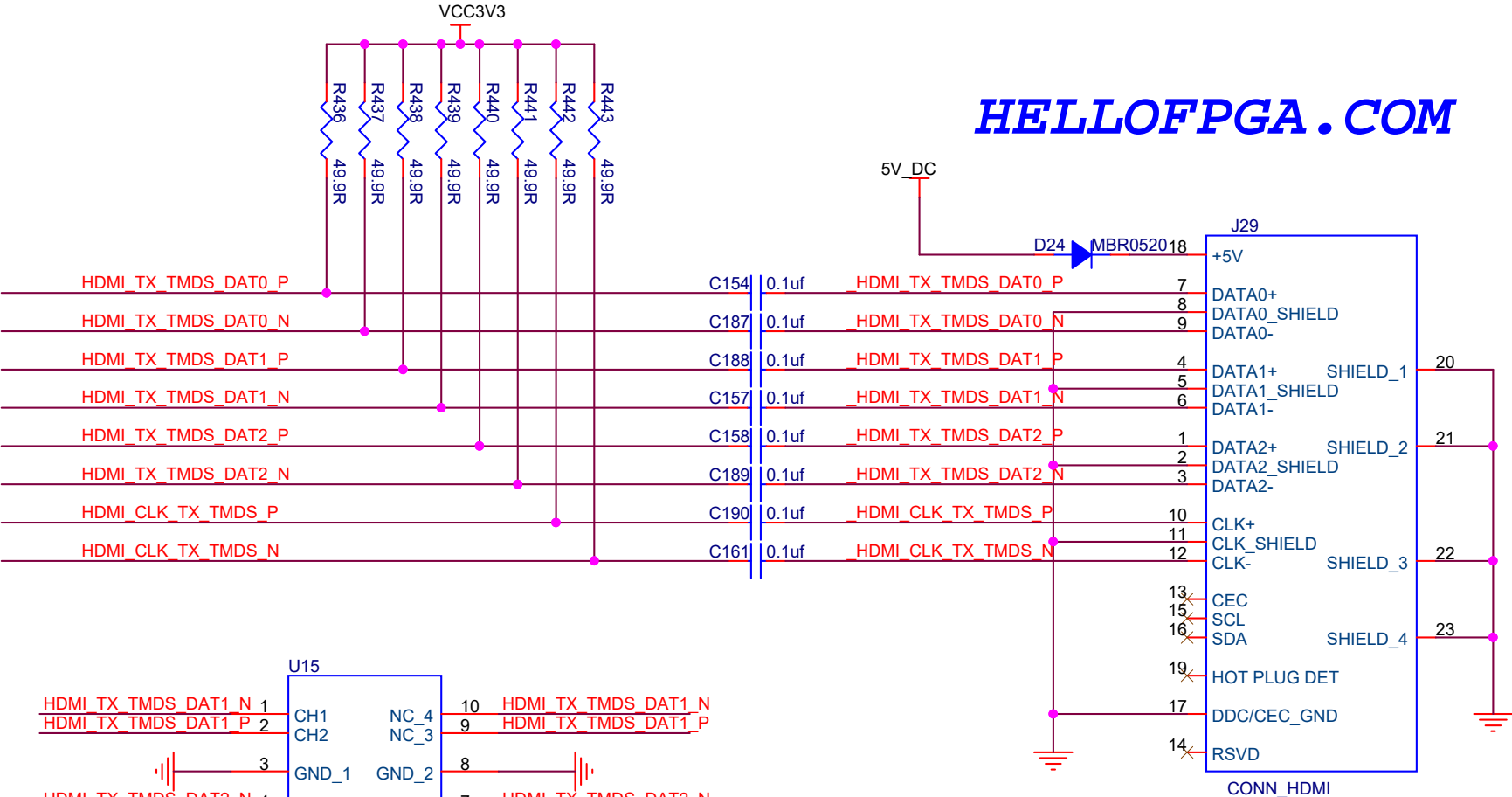


DDR PART

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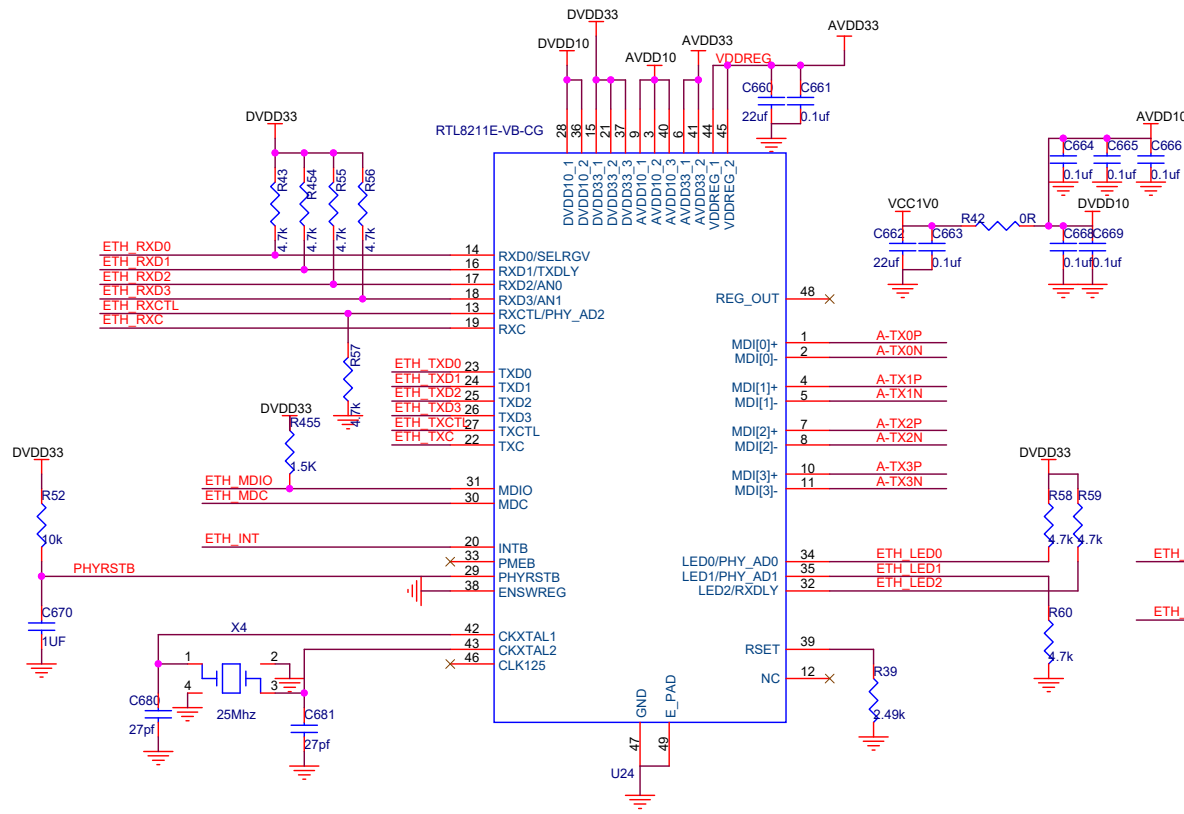
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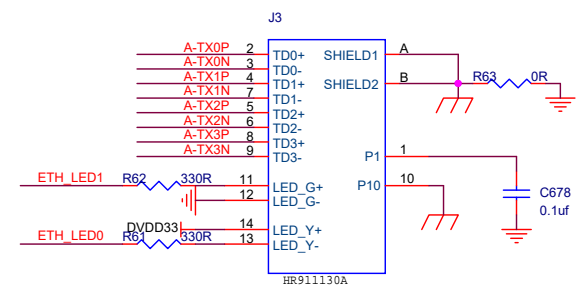


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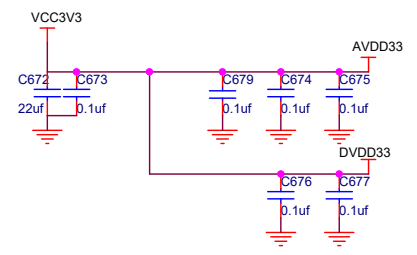
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NET PART

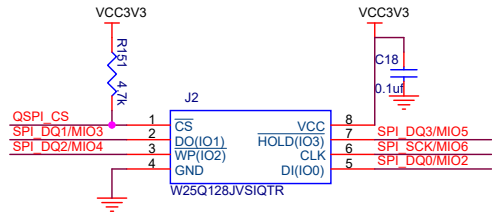


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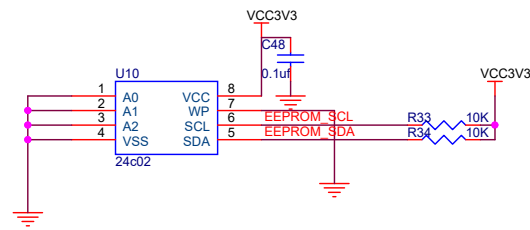


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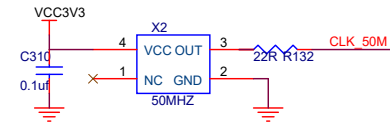
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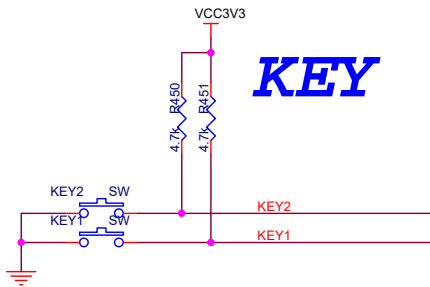
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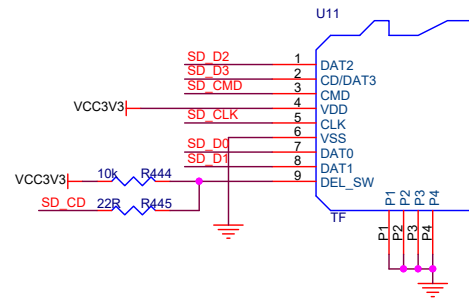
PL CLK



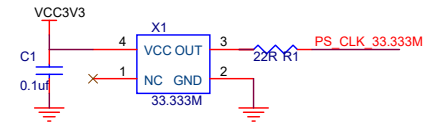
KEY



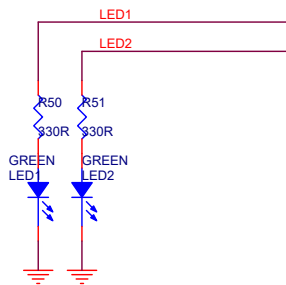
TF CARD



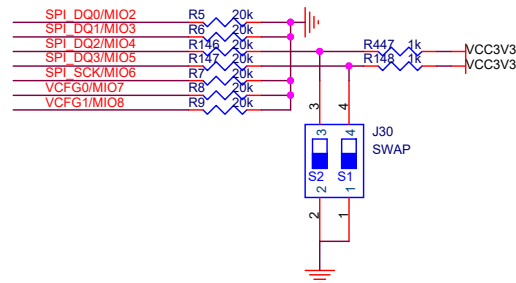
PS CLK



LED



BOOT

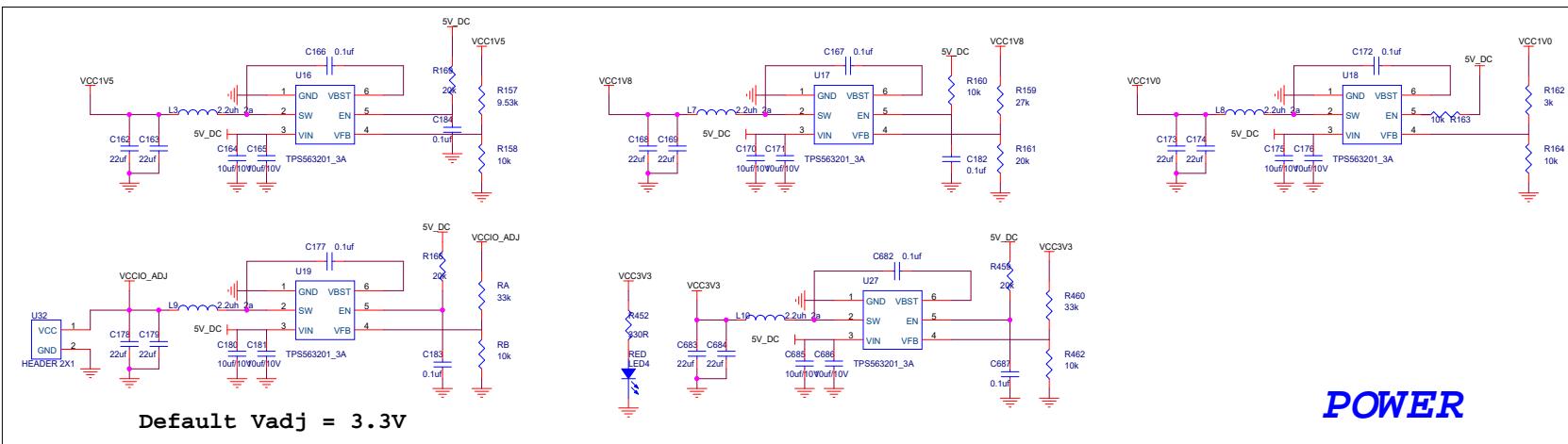


BOOT

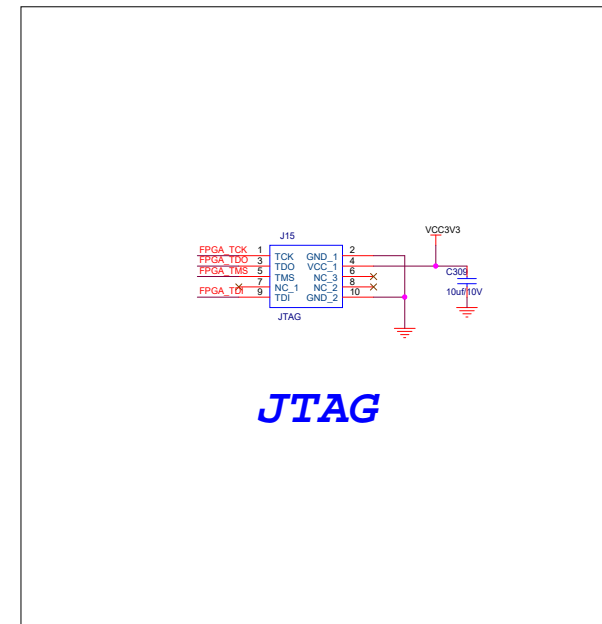
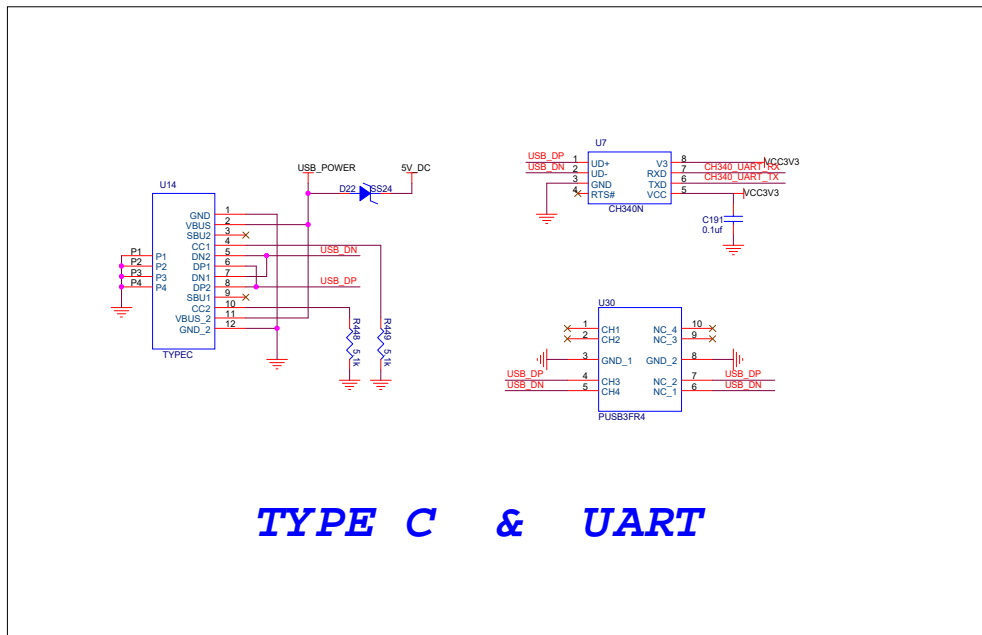
BOOT	S1	S2
JTAG	●	●
QSPI	○	●
SD	○	○

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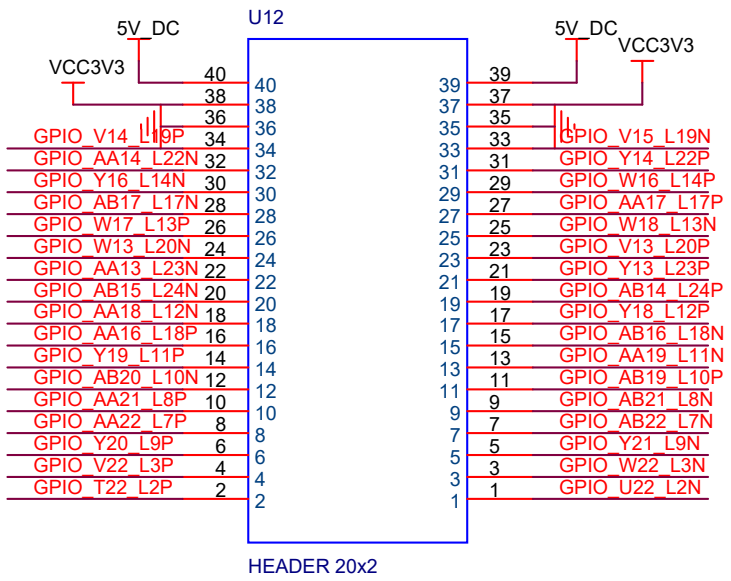
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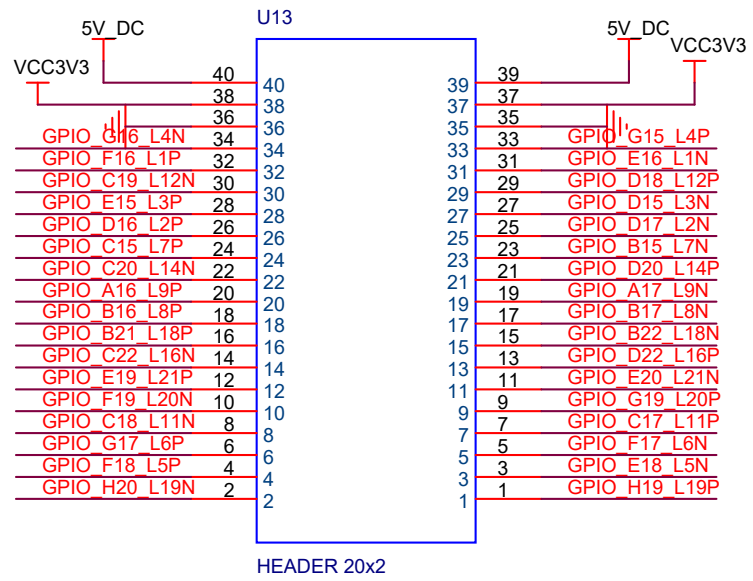


BANK 33



VCCIO :VADJ
Default Vadj = 3.3V

BANK 35



VCCIO :3.3V

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UART

ZYNQ_TX L17

ZYNQ_RX M17

EEPROM

SCL R20

SDA R21

50M CLOCK

CLK M19

KEY & LED

KEY1 K21

KEY2 J20

LED1 P20

LED2 P21

HDMI

CLK N22

D0 M21

D1 L21

D2 J21

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GigE phy

ETH TD0 E21

ETH TD1 F21

ETH TD2 F22

ETH TD3 G20

ETH TX_CTL G22

ETH TXC D21

ETH RD0 A22

ETH RD1 A18

ETH RD2 A19

ETH RD3 B20

ETH RX_CTL A21

ETH RXC B19

ETH MDIO H22

ETH MDC G21

ETH INT H18