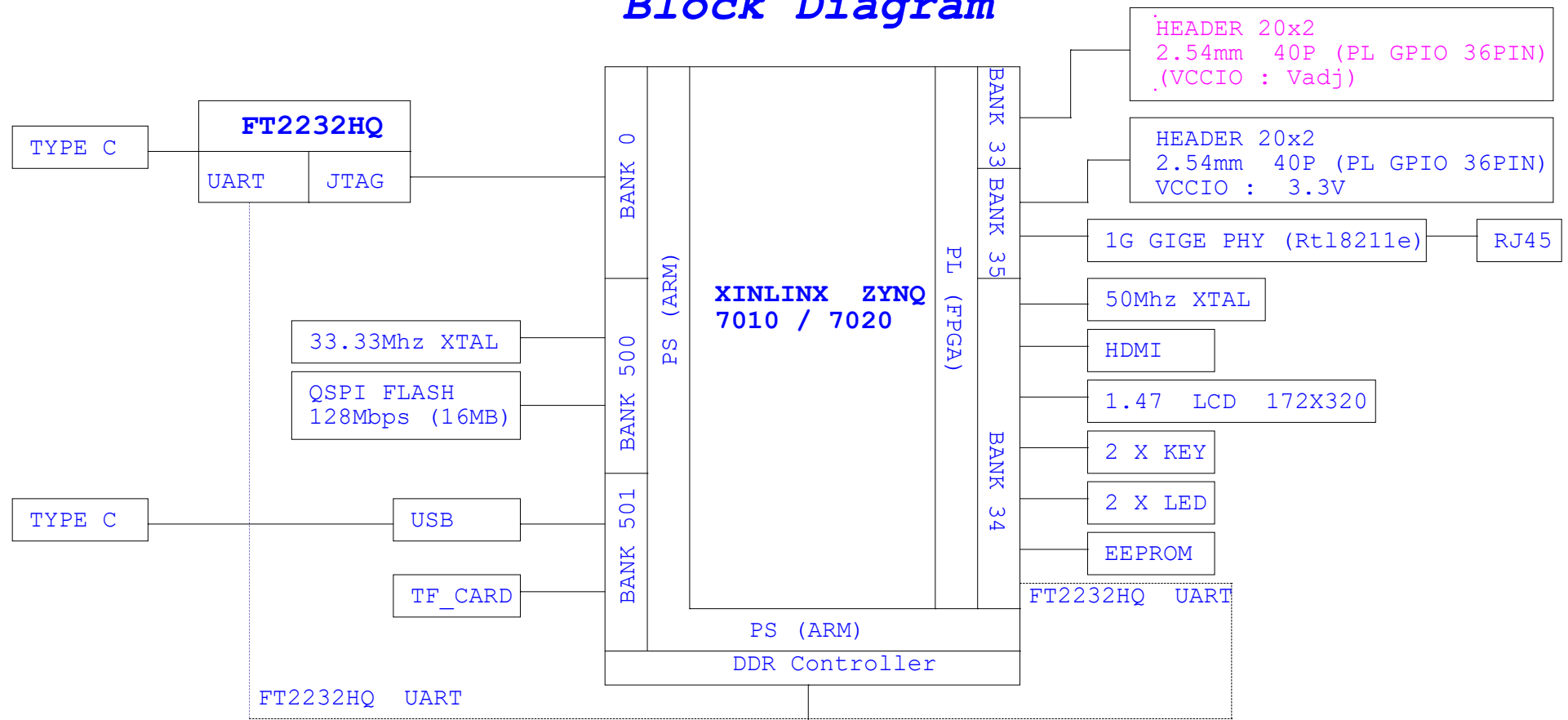


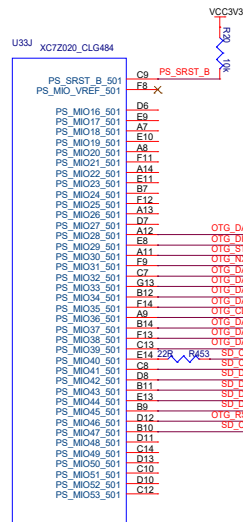
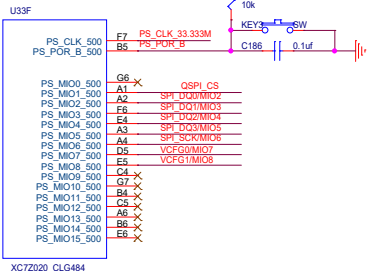
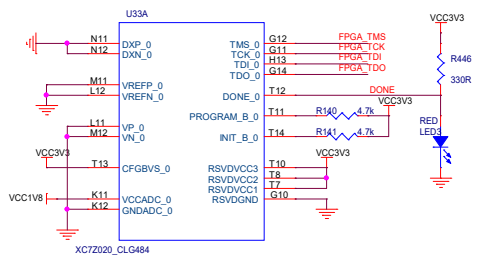
# Smart ZYNQ SP Block Diagram



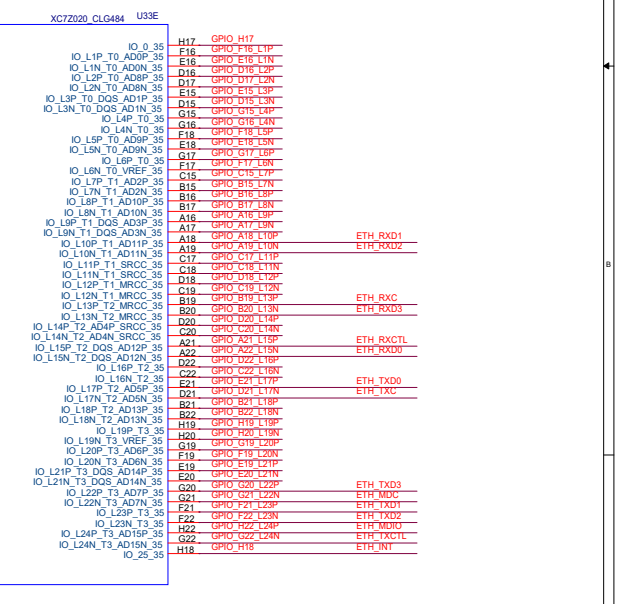
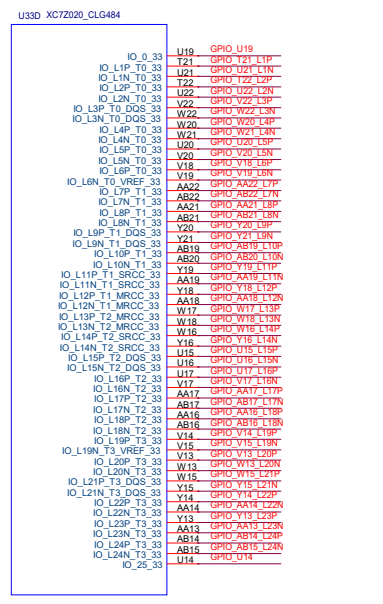
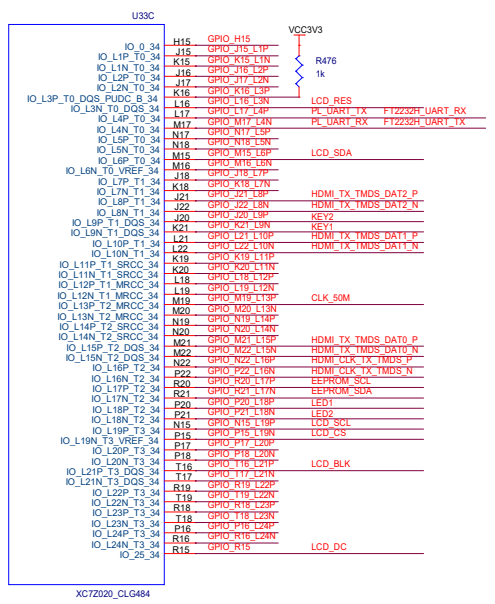
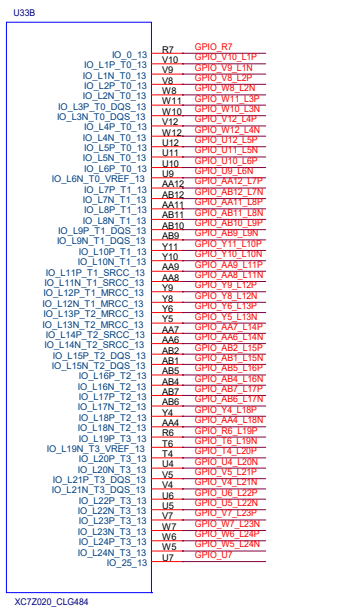
**VCCIO :** BANK 33 *Vadj (default 3.3V)*  
 BANK 34 **3.3V**  
 BANK 35 **3.3V**

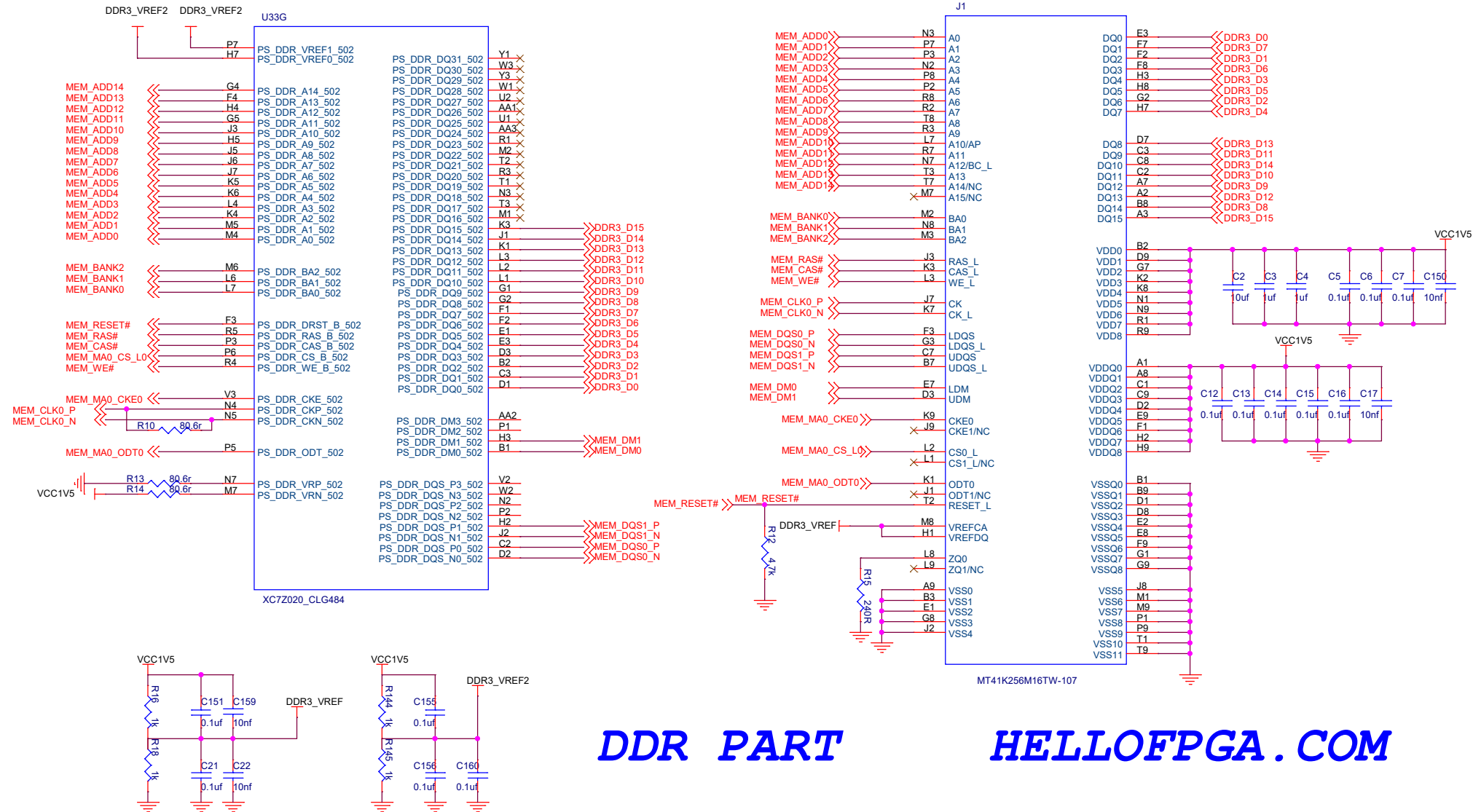
**MT41K256M16**  
 256M X 16bits  
 ( 512MB )

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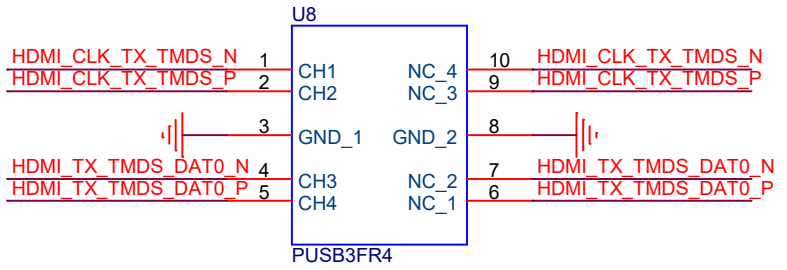
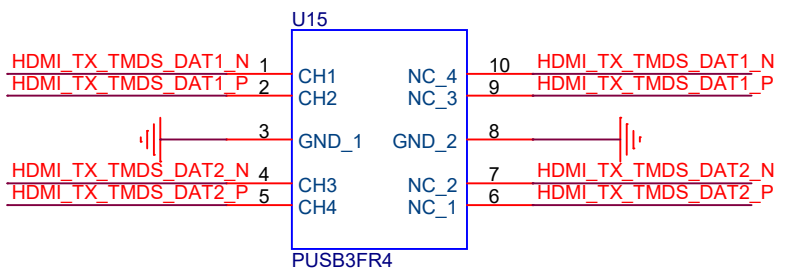
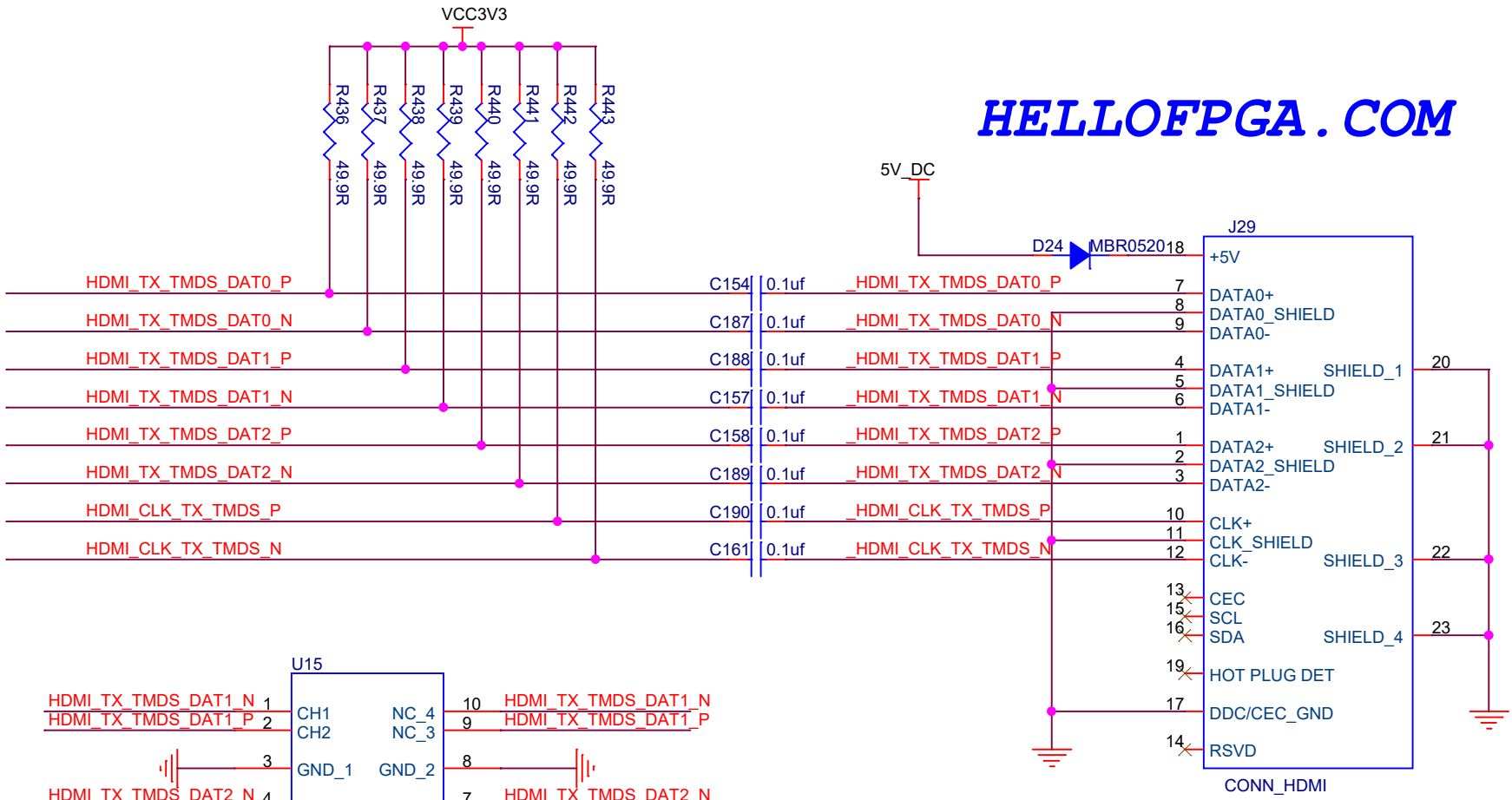


DDR PART

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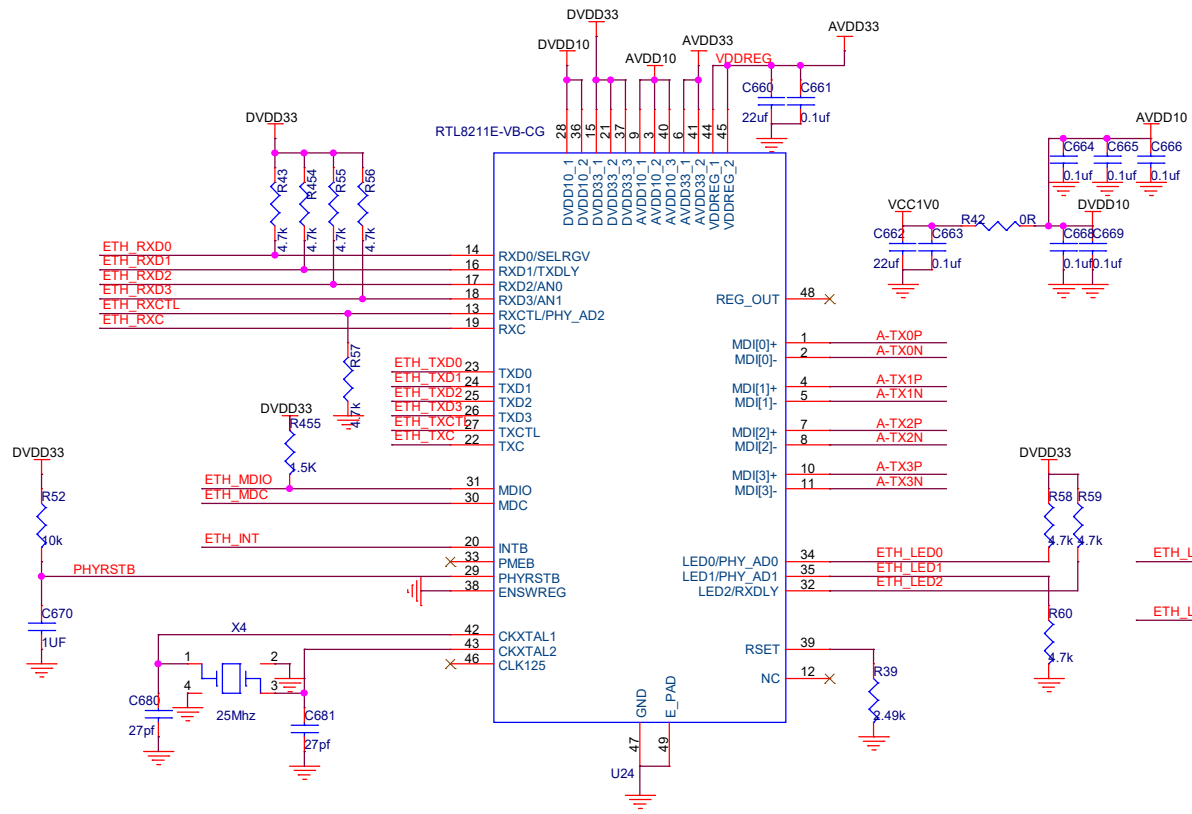
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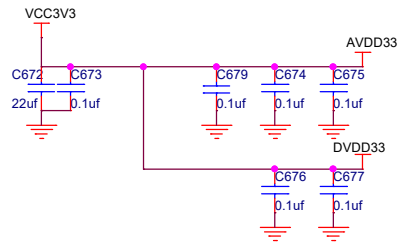
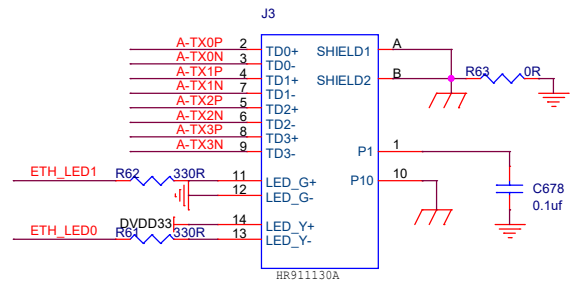


HDMI

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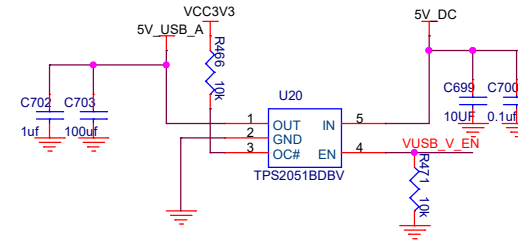
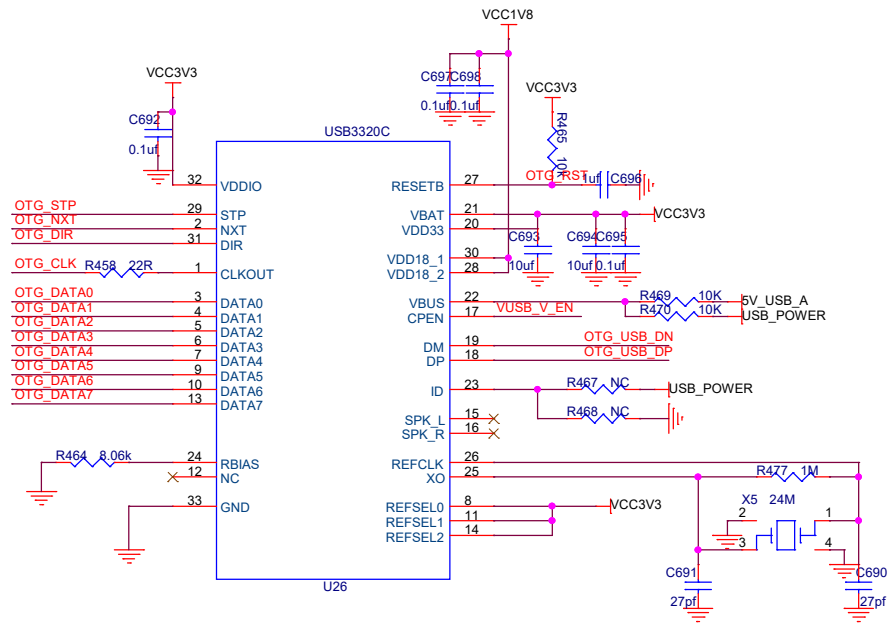


# NET PART

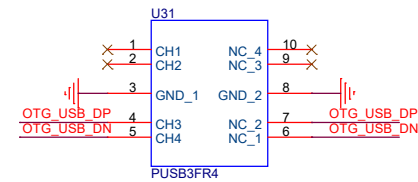
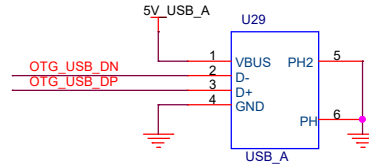
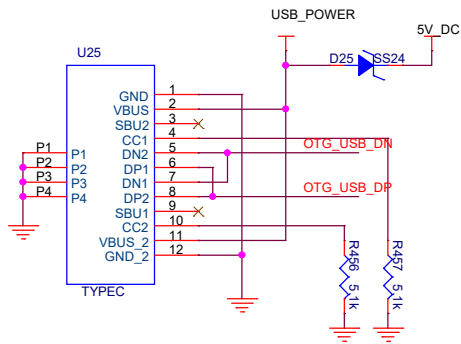


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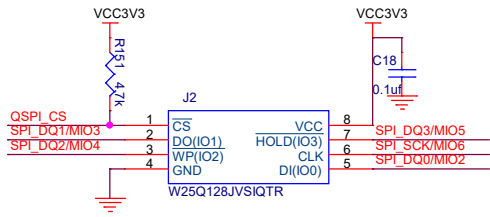
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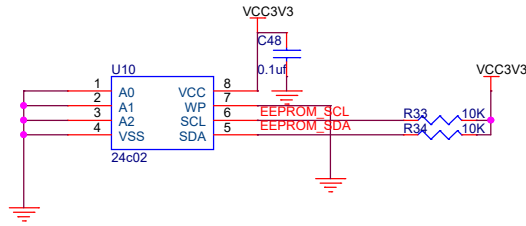
**USB PART**

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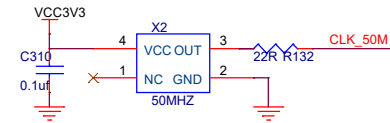
# QSPI FLASH



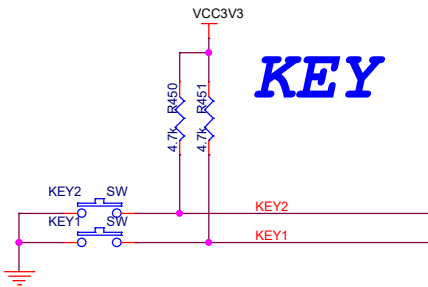
# EEPROM



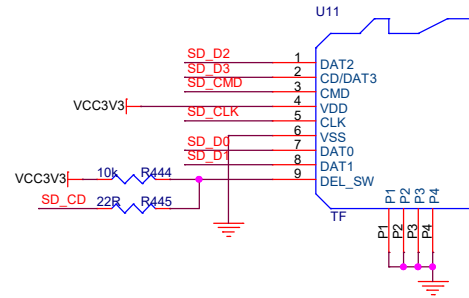
# PL CLK



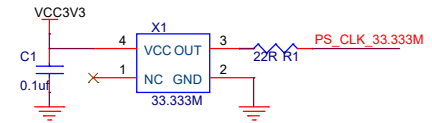
# KEY



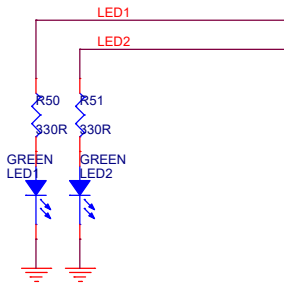
# TF CARD



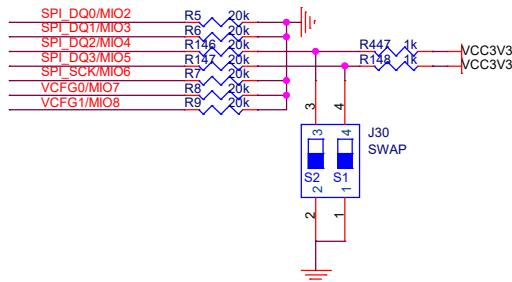
# PS CLK



# LED



# BOOT

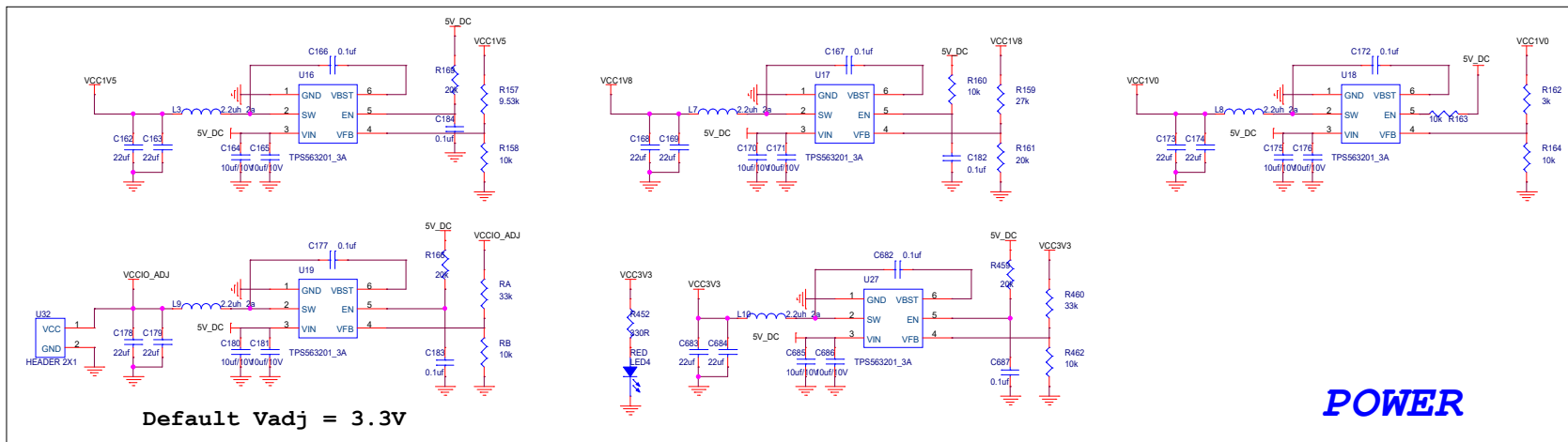


# BOOT

BOOT	S1	S2
JTAG	●	●
QSPI	○	●
SD	○	○

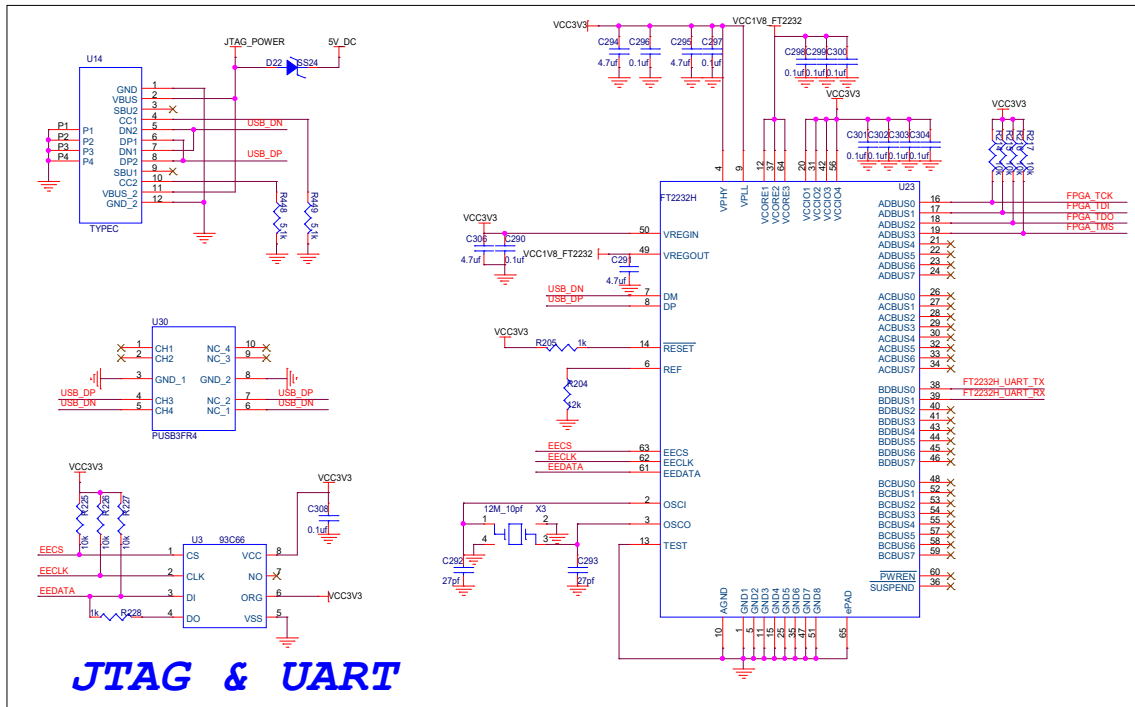
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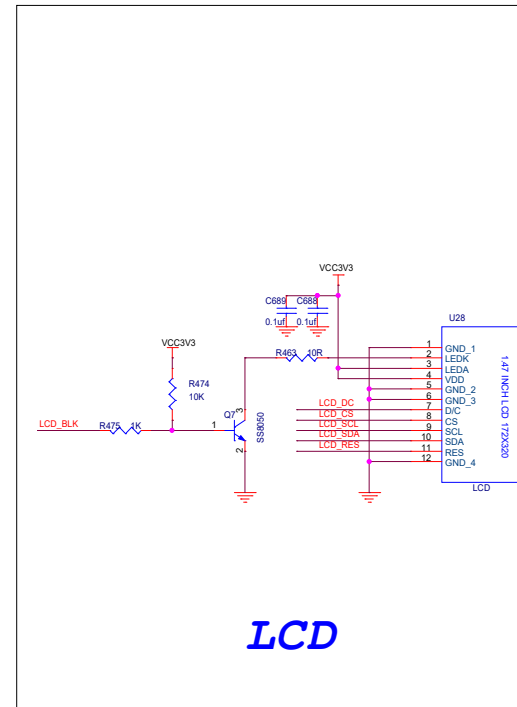


## POWER

# HELLOFPGA.COM

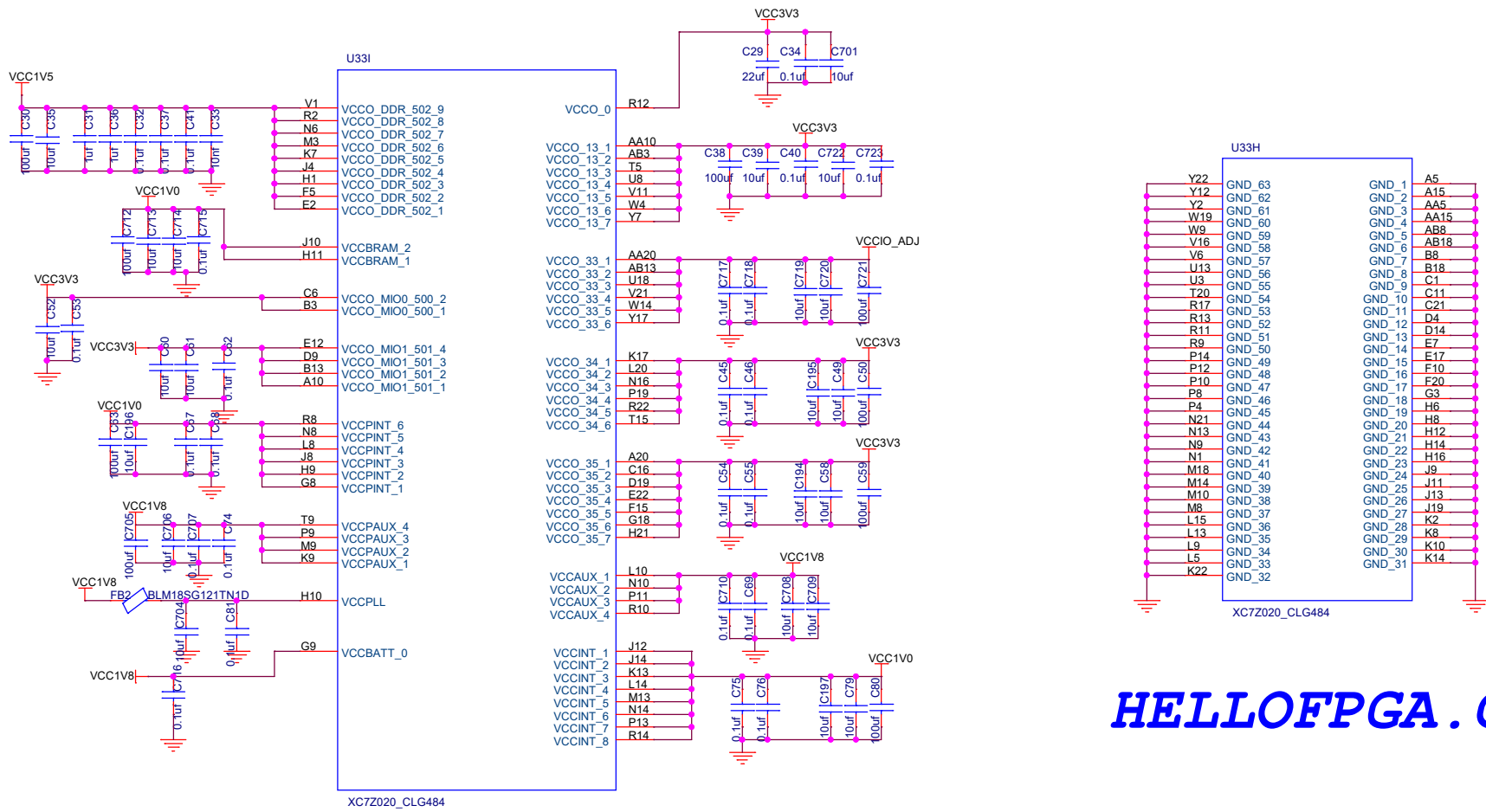


## JTAG & UART



## LCD

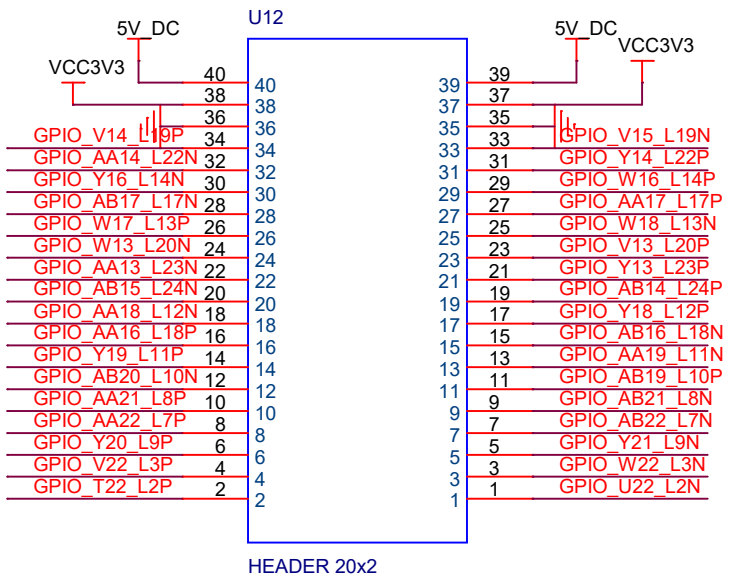




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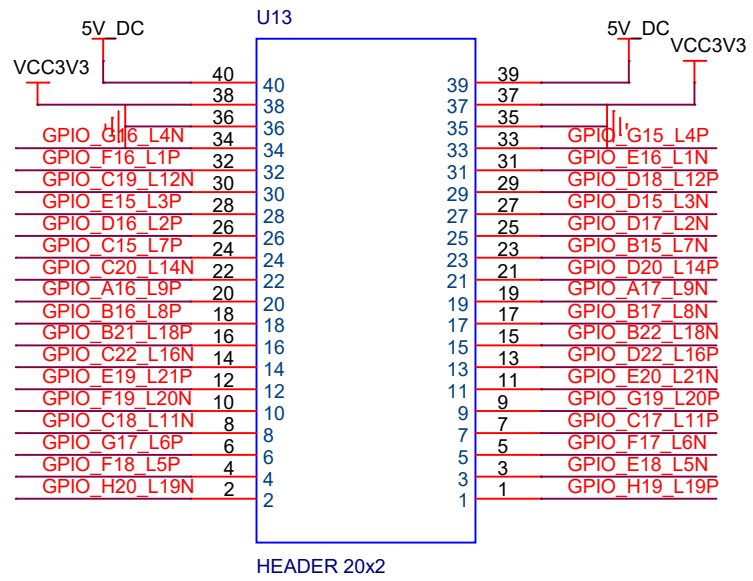
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### BANK 33



VCCIO :VADJ  
Default Vadj = 3.3V

### BANK 35



VCCIO :3.3V

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### **HDMI**

CLK	N22
D0	M21
D1	L21
D2	J21

### **UART**

ZYNQ_TX	L17
ZYNQ_RX	M17

### **EEPROM**

SCL	R20
SDA	R21

### **50M CLOCK**

CLK	M19
-----	-----

### **KEY & LED**

KEY1	K21
KEY2	J20
LED1	P20
LED2	P21

### **LCD 320X172**

LCD_DC	R15
LCD_CS	P15
LCD_SCL	N15
LCD_SDA	M15
LCD_RES	L16
LCD_BLK	T16

(LCD BLK : default high level by  
External pull-up resistance )

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### **GigE phy**

ETH TD0	E21
ETH TD1	F21
ETH TD2	F22
ETH TD3	G20
ETH TX_CTL	G22
ETH TXC	D21
ETH RD0	A22
ETH RD1	A18
ETH RD2	A19
ETH RD3	B20
ETH RX_CTL	A21
ETH RXC	B19
ETH MDIO	H22
ETH MDC	G21
ETH INT	H18