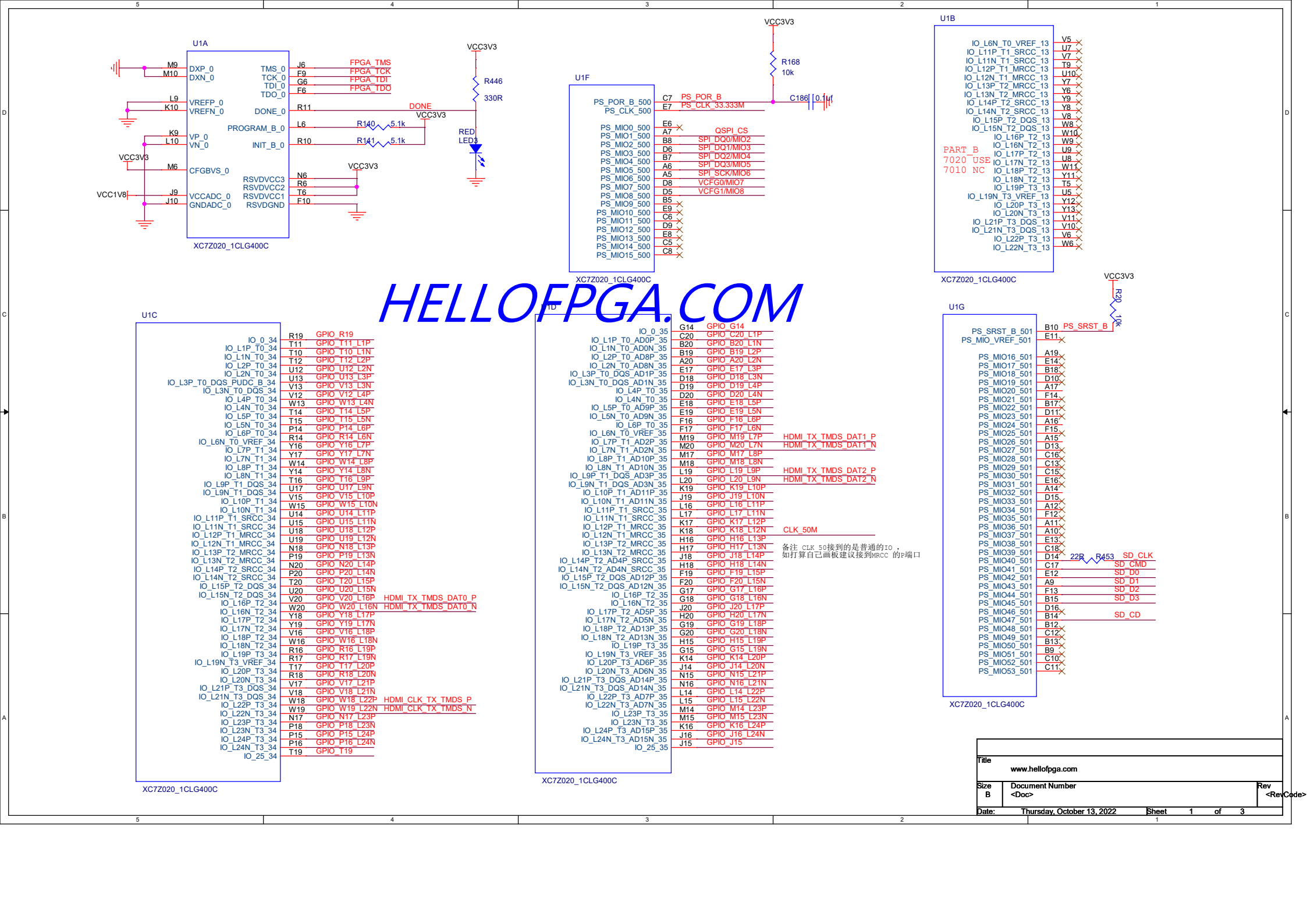
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M10
DXP_0
DXN_0
L9
K10
VREFP_0
VREFN_0
K9
L10
VP_0
VN_0
VCC3V3
M6
CFGBVS_0
VCC1V8
J9
J10
VCCADC_0
GNDADC_0
TMS_0
TCK_0
TDI_0
TDO_0
DONE_0
PROGRAM_B_0
INIT_B_0
RSVDVCC3
RSVDVCC2
RSVDVCC1
RSVDGND
J6
F9
G6
F6
R11
L6
R10
N6
R6
T6
F10
FPGA_TMS
FPGA_TCK
FPGA_TDI
FPGA_TDO
DONE
R140
5.1k
R141
5.1k
VCC3V3
R446
330R
RED
LED3
XC7Z020_1CLG400C
U1F
PS_POR_B_500
PS_CLK_500
PS_MIO0_500
PS_MIO1_500
PS_MIO2_500
PS_MIO3_500
PS_MIO4_500
PS_MIO5_500
PS_MIO6_500
PS_MIO7_500
PS_MIO8_500
PS_MIO9_500
PS_MIO10_500
PS_MIO11_500
PS_MIO12_500
PS_MIO13_500
PS_MIO14_500
PS_MIO15_500
C7
E7
E6
A7
B8
D6
B7
A6
A5
D8
D5
B5
E9
C6
D9
E8
C5
C8
PS_POR_B
PS_CLK_33.333M
QSPI_CS
SPI_DQ0/MIO2
SPI_DQ1/MIO3
SPI_DQ2/MIO4
SPI_DQ3/MIO5
SPI_SCK/MIO6
VCFG0/MIO7
VCFG1/MIO8
VCC3V3
R168
10k
C186
0.1uf
XC7Z020_1CLG400C
U1B
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IO_L11P_T1_SRCC_13
IO_L11N_T1_SRCC_13
IO_L12P_T1_MRCC_13
IO_L12N_T1_MRCC_13
IO_L13P_T2_MRCC_13
IO_L13N_T2_MRCC_13
IO_L14P_T2_SRCC_13
IO_L14N_T2_SRCC_13
IO_L15P_T2_DQS_13
IO_L15N_T2_DQS_13
IO_L16P_T2_13
IO_L16N_T2_13
IO_L17P_T2_13
IO_L17N_T2_13
IO_L18P_T2_13
IO_L18N_T2_13
IO_L19P_T3_13
IO_L19N_T3_VREF_13
IO_L20P_T3_13
IO_L20N_T3_13
IO_L21P_T3_DQS_13
IO_L21N_T3_DQS_13
IO_L22P_T3_13
IO_L22N_T3_13
V5
U7
V7
T9
U10
Y7
Y6
Y9
Y8
V8
W8
W10
W9
U9
U8
W11
Y11
T5
U5
Y12
Y13
V11
V10
V6
W6
PART_B
7020 USE
7010 NC
XC7Z020_1CLG400C
U1C
IO_0_34
IO_L1P_T0_34
IO_L1N_T0_34
IO_L2P_T0_34
IO_L2N_T0_34
IO_L3P_T0_DQS_PUDC_B_34
IO_L3N_T0_DQS_34
IO_L4P_T0_34
IO_L4N_T0_34
IO_L5P_T0_34
IO_L5N_T0_34
IO_L6P_T0_34
IO_L6N_T0_VREF_34
IO_L7P_T1_34
IO_L7N_T1_34
IO_L8P_T1_34
IO_L8N_T1_34
IO_L9P_T1_DQS_34
IO_L9N_T1_DQS_34
IO_L10P_T1_34
IO_L10N_T1_34
IO_L11P_T1_SRCC_34
IO_L11N_T1_SRCC_34
IO_L12P_T1_MRCC_34
IO_L12N_T1_MRCC_34
IO_L13P_T2_MRCC_34
IO_L13N_T2_MRCC_34
IO_L14P_T2_SRCC_34
IO_L14N_T2_SRCC_34
IO_L15P_T2_DQS_34
IO_L15N_T2_DQS_34
IO_L16P_T2_34
IO_L16N_T2_34
IO_L17P_T2_34
IO_L17N_T2_34
IO_L18P_T2_34
IO_L18N_T2_34
IO_L19P_T3_34
IO_L19N_T3_VREF_34
IO_L20P_T3_34
IO_L20N_T3_34
IO_L21P_T3_DQS_34
IO_L21N_T3_DQS_34
IO_L22P_T3_34
IO_L22N_T3_34
IO_L23P_T3_34
IO_L23N_T3_34
IO_L24P_T3_34
IO_L24N_T3_34
IO_25_34
R19
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P16
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GPIO_V13_L3N
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GPIO_W19_L22N
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GPIO_P18_L23N
GPIO_P15_L24P
GPIO_P16_L24N
GPIO_T19
HDMI_TX_TMDS_DAT0_P
HDMI_TX_TMDS_DAT0_N
HDMI_CLK_TX_TMDS_P
HDMI_CLK_TX_TMDS_N
XC7Z020_1CLG400C
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IO_L1P_T0_AD0P_35
IO_L1N_T0_AD0N_35
IO_L2P_T0_AD8P_35
IO_L2N_T0_AD8N_35
IO_L3P_T0_DQS_AD1P_35
IO_L3N_T0_DQS_AD1N_35
IO_L4P_T0_35
IO_L4N_T0_35
IO_L5P_T0_AD9P_35
IO_L5N_T0_AD9N_35
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IO_L11N_T1_SRCC_35
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GPIO_L15_L22N
GPIO_M14_L23P
GPIO_M15_L23N
GPIO_K16_L24P
GPIO_J16_L24N
GPIO_J15
HDMI_TX_TMDS_DAT1_P
HDMI_TX_TMDS_DAT1_N
HDMI_TX_TMDS_DAT2_P
HDMI_TX_TMDS_DAT2_N
CLK_50M
备注 CLK_50接到的是普通的IO，
如打算自己画板建议接到MRCC 的P端口
XC7Z020_1CLG400C
U1G
PS_SRST_B_501
PS_MIO_VREF_501
PS_MIO16_501
PS_MIO17_501
PS_MIO18_501
PS_MIO19_501
PS_MIO20_501
PS_MIO21_501
PS_MIO22_501
PS_MIO23_501
PS_MIO24_501
PS_MIO25_501
PS_MIO26_501
PS_MIO27_501
PS_MIO28_501
PS_MIO29_501
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F14
B17
D11
A16
F15
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C16
C13
C15
E16
A14
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A11
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E13
C18
D14
C17
E12
A9
F13
B15
D16
B14
B12
C12
B13
B9
C10
C11
PS_SRST_B
R20
10k
22R
R453
SD_CLK
SD_CMD
SD_D0
SD_D1
SD_D2
SD_D3
SD_CD
XC7Z020_1CLG400C
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Rev
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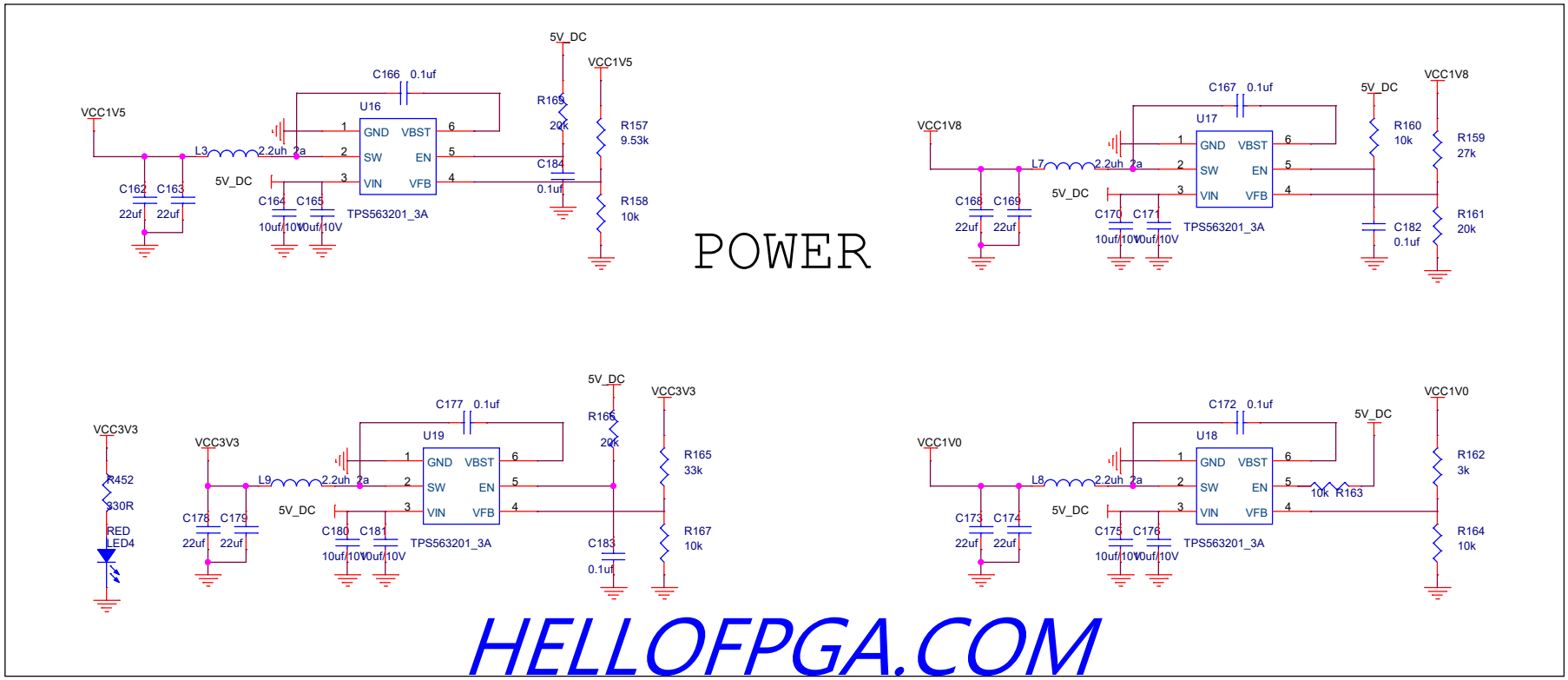

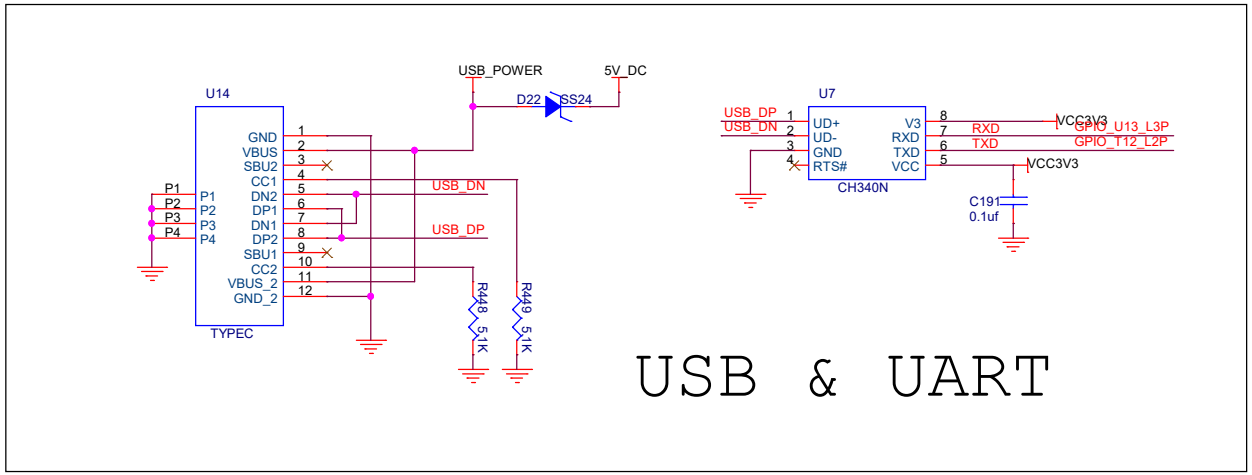

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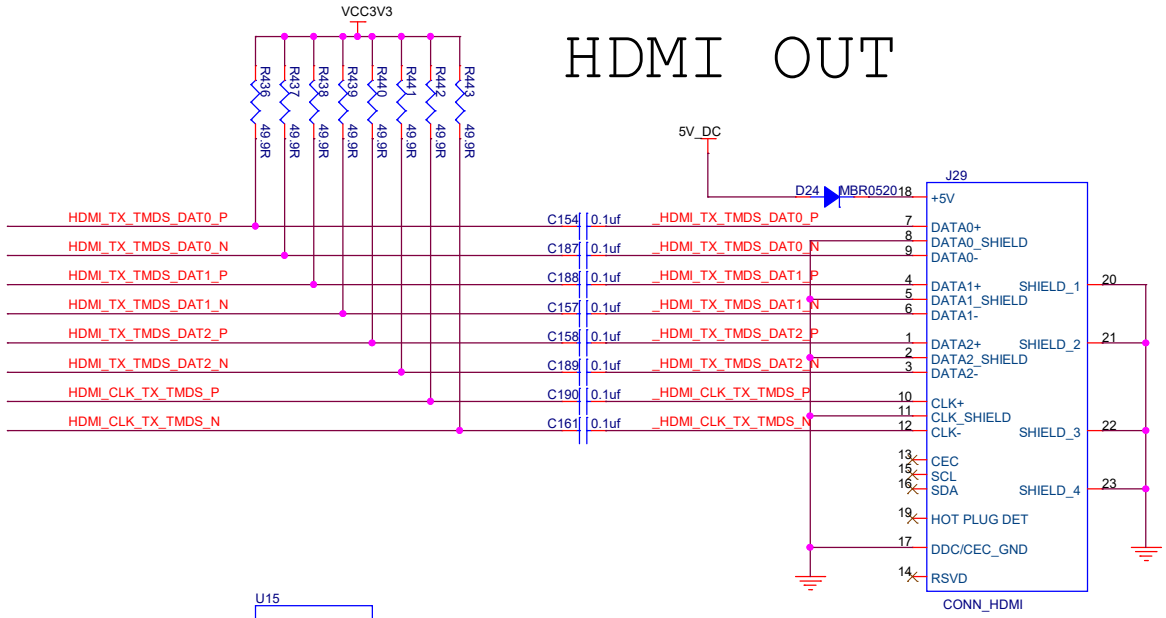

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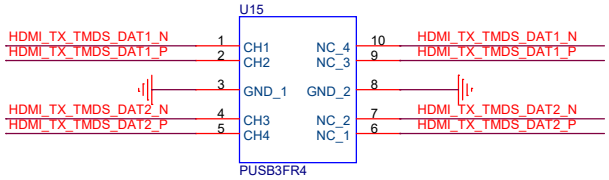

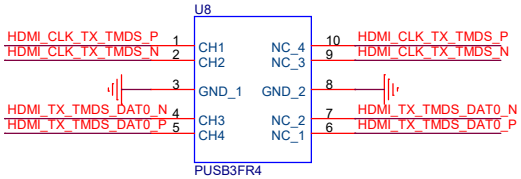

HDMI ESD

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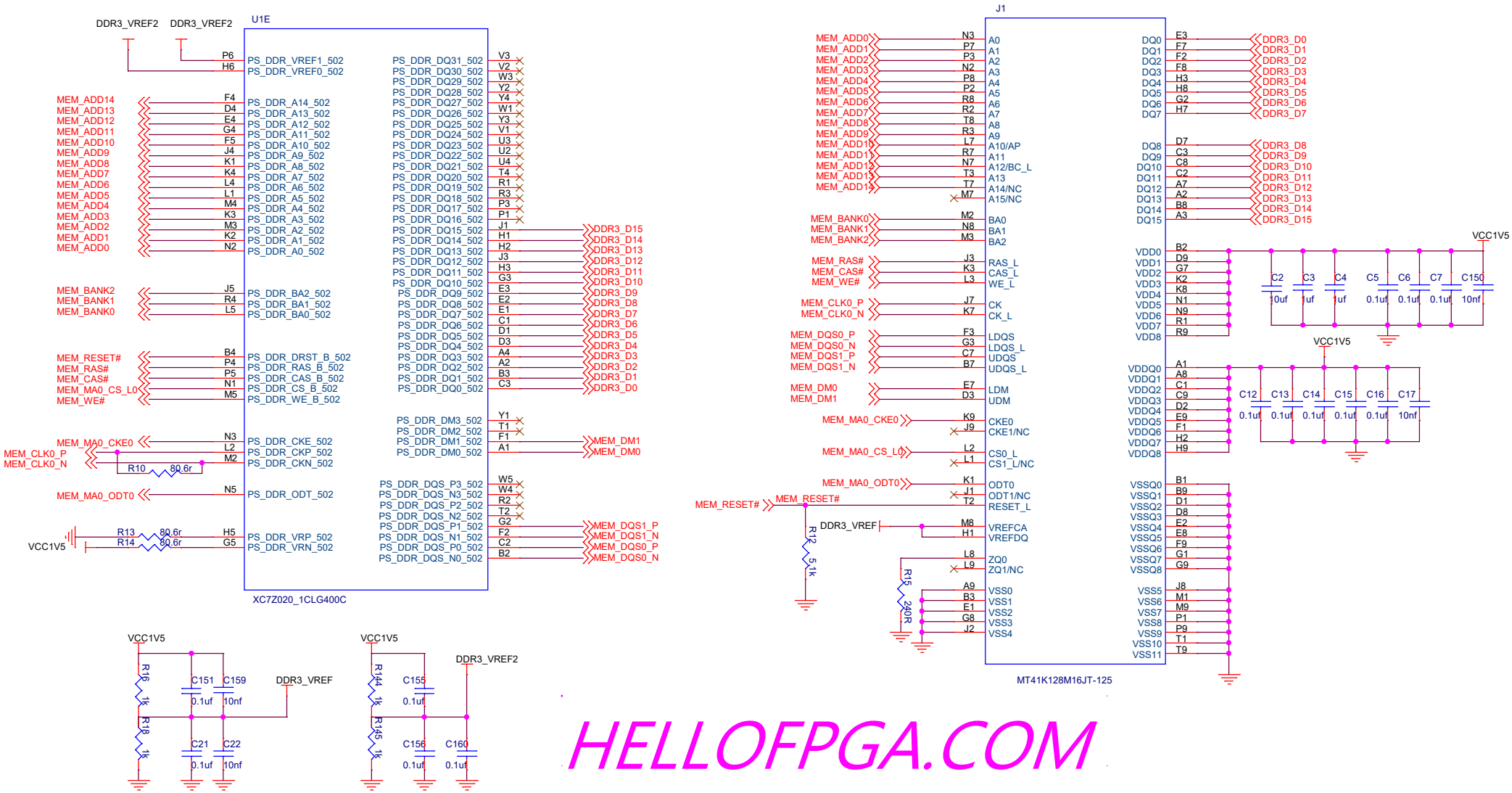
DDR PART



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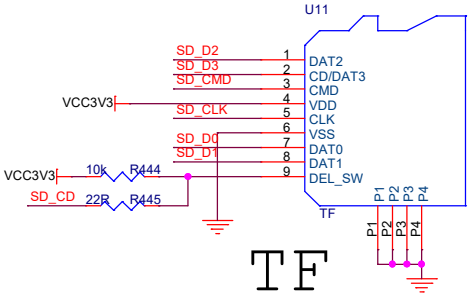

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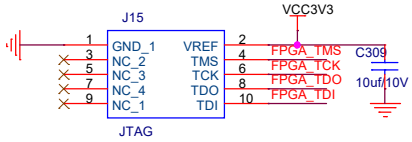

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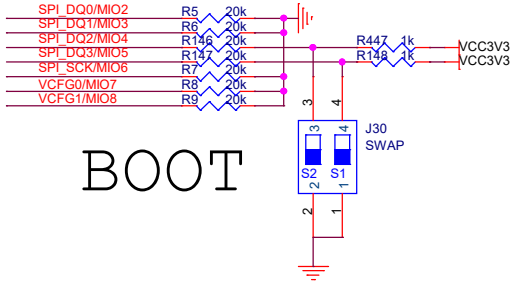
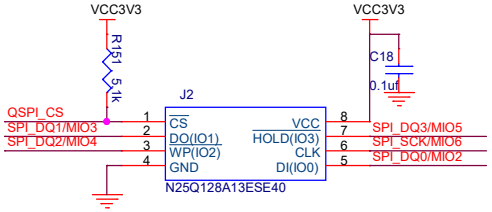


BOOT

BOOT	S1	S2
JTAG	●	●
QSPI	○	●
SD	○	○

ON ● OFF ○



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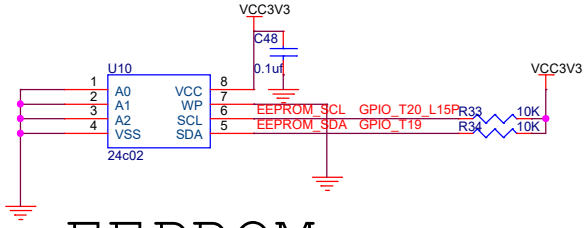

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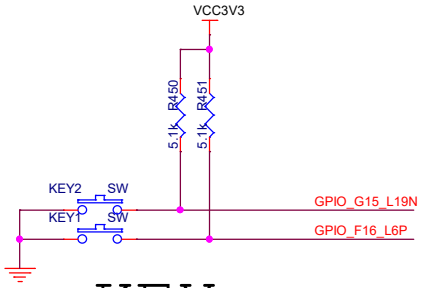

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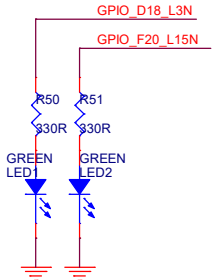
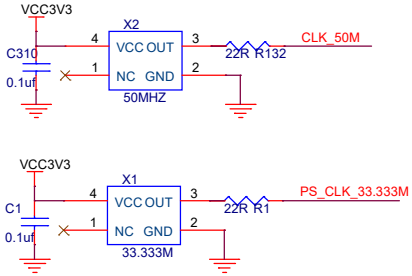


LED



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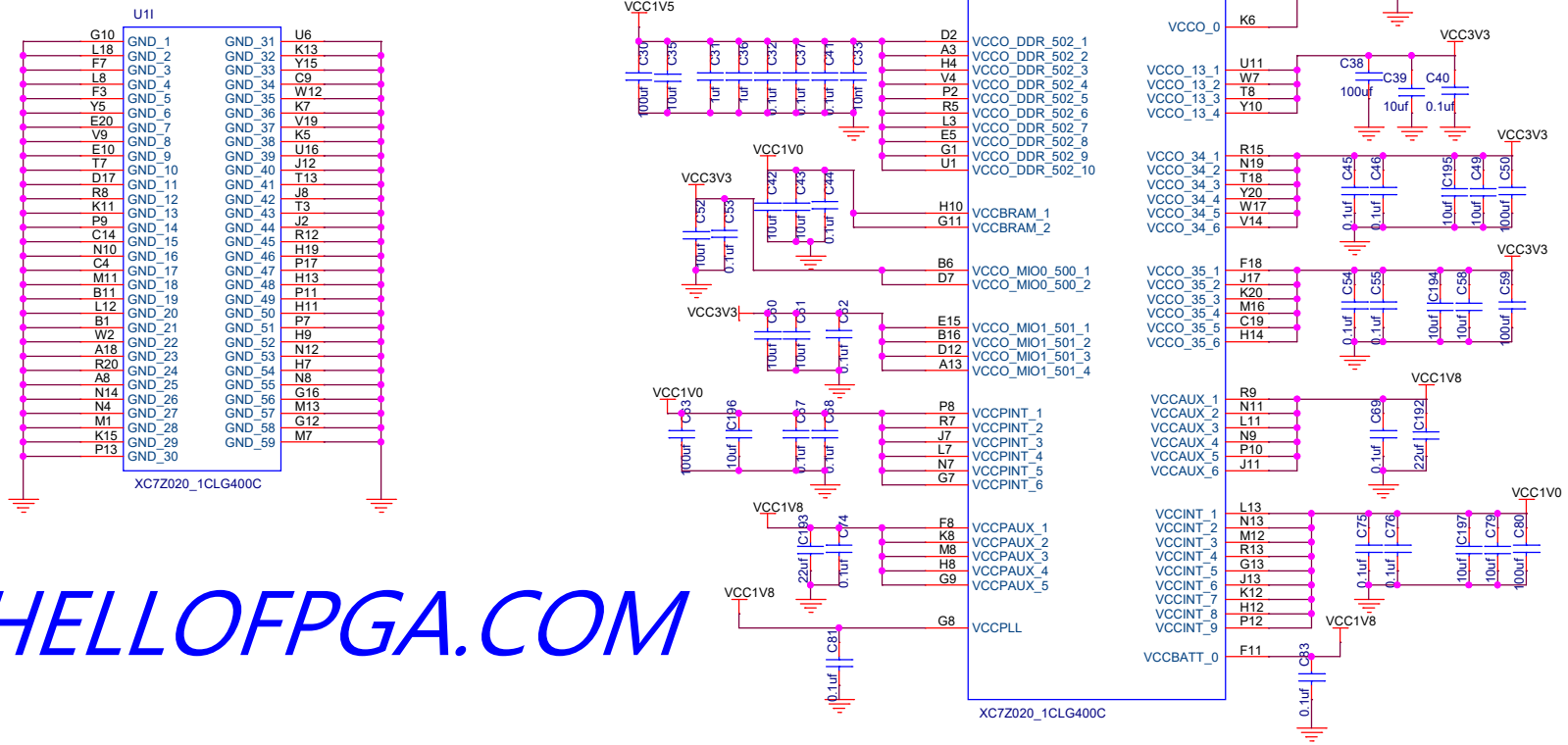

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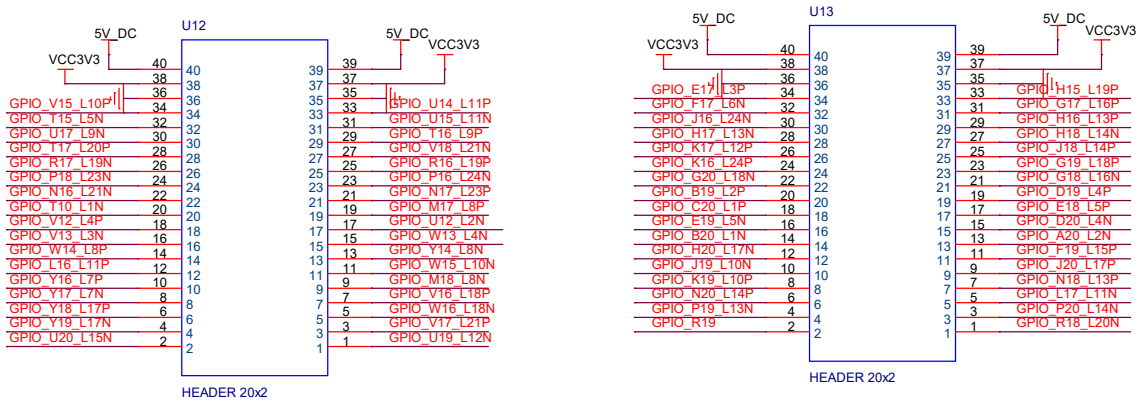

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